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**FLIP-CHIP FABRICATION OF ADVANCED  
MICROELECTROMECHANICAL SYSTEMS  
AND INTEGRATED MICROSYSTEMS**

by

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B. S. Space Physics, United States Air Force Academy, 1993  
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FLIP-CHIP FABRICATION OF ADVANCED MICROELECTROMECHANICAL  
SYSTEMS AND INTEGRATED MICROSYSTEMS

THESIS DIRECTED BY ASSOCIATE PROFESSOR VICTOR M. BRIGHT

## **ABSTRACT**

One of the most enabling features of any Microelectromechanical Systems (MEMS) fabrication service is the number of structural layers available to the designer of surface-micromachined components. The complexity and capabilities of such devices increases significantly with the number of structural layers since more intricate mechanisms can be created and there are more choices in the thickness and height of any desired structure. Commercial foundries, however, limit designers to very few choices of materials or number of structural layers. As a result, it may not be possible to create many specialized devices required for more demanding applications without custom fabrication methods which are usually very expensive.

As an alternative, this research has demonstrated a novel, simple, repeatable, reliable, and inexpensive post-process flip-chip assembly technique that was developed to use existing fabrication processes. Commercial foundries have fully optimized fabrication for increased yield, turn-around time, and reduced cost. Therefore, rather than develop an entirely new method of fabrication, the flip-chip assembly technique leverages the existing industry and is far more efficient and realizable. Highly complex structures and integrated microsystems can be made by

flip-chip bonding surface-micromachined features onto a variety of other work surfaces like ceramic substrates, CMOS control chips or even other MEMS chips fabricated in the same process. The original silicon host substrate is then removed during the release etch to produce highly advanced systems that are better suited to RF, microwave, or optical applications where specific material properties, additional layers or control electronics are required.

This dissertation presents the design, commercial prefabrication, flip-chip assembly, modeling and testing of highly advanced MEMS and integrated microsystems such as numerous styles of piston, torsion and cantilever micromirror arrays as well as other demonstration devices like variable capacitors, VCSEL integration reflectors and mechanical transistors and relays. All devices boast unprecedented features compared to conventional fabrication or were uniquely enabled by the flip-chip fabrication process.

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# CHAPTER 1

## INTRODUCTION

The research presented in this document spans two separate research projects that sought to create advanced microelectromechanical systems (MEMS) intended for use in specific and highly demanding applications. The first effort was to produce a variety of variable capacitors suitable for radio frequency (RF) applications of miniaturized electronics. The second was to create advanced micromirror arrays integrated with complementary metal-oxide-semiconductor (CMOS) electronics for optical switching applications. Although both projects were distinct in virtually every aspect of design, modeling, testing and final implementation, the means to fabricate such devices became increasingly similar.

By working both projects, the lessons learned from one were applied to the other until a broad method of flip-chip fabrication was developed. The flip-chip fabrication process has routinely demonstrated a unique and yet flexible means to create a wide variety of advanced MEMS and integrated microsystems. As a result, this document has evolved largely into a report of a new fabrication technology rather than a report of the development of two separate forms of devices. Although the demonstration of such a flip-chip fabrication technology involves these devices, the primary focus of this document is to report the novel, inexpensive, fast and often quite simple and reliable means to fabricate them.



## **1.1 Purpose of Research**

This research began as an effort to fabricate flip-chip variable capacitors atop ceramic substrates to improve the RF performance of highly miniaturized tunable transceivers. Due to adverse charging effects of the silicon substrates used in standard surface-micromachining services, traditional fabrication of variable capacitors simply would not achieve the performance required for the intended applications. Current fabrication methods simply pose too many adverse characteristics for RF applications that are too severe to overcome by design. The only alternative was to create a new method of fabrication which enables the use of surface-micromachined components fabricated atop selected substrates that are far better suited to demanding RF applications.

The initial flip-chip assembly process was developed for this reason. This technique enabled the transfer of MEMS components from standard commercial foundry services to ceramic substrates on which a single layer of gold could be patterned for wiring and electrical shielding. Although a sometimes low yield process, this technique demonstrated that such flip-chip fabrication of MEMS structures suitable for RF applications was possible. The project quickly progressed into an effort to combine optimal design with manufacturability using the flip-chip process. This promising research is still an ongoing effort within the department.

Once the flip-chip fabrication process had been demonstrated with the variable capacitors, it was quickly realized that this process could be used to transfer the same structures to other work surfaces. Since flip-chip structures are inherently planarized, many potential customers sought a means to fabricate optical components

using a similar method. In particular, this process uniquely enabled the fabrication of surface-micromachined micromirror devices atop CMOS control electronics. Similar devices had been fabricated in recent years at incredible expense using a custom foundry service that will not likely become commercially available [1]. The flip-chip method allows the creation of very similar devices, but at remarkably lower cost since existing commercial foundry services are available for prefabrication of flip-chip components. As a result, a second project began with the goal to produce large arrays of cantilever micromirror devices atop CMOS control electronics for optical switching and scanning applications.

## **1.2 Scope of Research**

Although the flip-chip fabrication of advanced MEMS and integrated microsystems has been routinely demonstrated throughout the course of this research, numerous questions remain regarding the fundamental mechanisms of flip-chip bonding between a variety of materials. Likewise, each type of bond is a function of numerous variables such as temperature, bonding stress, ultrasonic energy, bond time and still more variables surrounding the size, distribution, quantity and geometric shape of bond pads. With each question that was answered by experimental data, still more arose until it became evident that each study of any one particular configuration of flip-chip bonding became sufficient to support an entire course of research. As a result, the scope of this research does not seek to answer all fundamental issues regarding the mechanical, chemical or electrical principles of the flip-chip bonding

process. Instead, this research has evolved into a means to develop and demonstrate a variety of flip-chip fabrication techniques that uniquely solve critical problems specific to demanding applications in a variety of fields. This research demonstrates the flip-chip assembly of advanced MEMS on ceramic substrates, CMOS electronics and other MEMS substrates in which all cases have produced novel devices that were uniquely enabled by the new method of fabrication.

The flip-chip assembly research presented in this document is divided into four specific categories. In all cases, polysilicon structures are prefabricated in a commercial surface-micromachining process and then bonded to a desired work surface. First, these structures are bonded to a ceramic substrate patterned in gold. As previously mentioned, this technique was originally designed to fabricate RF components, but has since been adapted to enable the other categories of flip-chip assembly. In the second category, the polysilicon structures are flip-chip bonded to a “submount” receiving chip that is also fabricated in the same surface-micromachining process. This technique enables highly complex polysilicon structures. The third category is very similar except the structures and submount features are fabricated on the same chip. This monolithic approach to the flip-chip assembly technique creates highly complex polysilicon structures without the need for most of the preprocessing steps. Finally, the last category involves transferring polysilicon structures to CMOS chips in a manner that creates complex devices on the same chip as control electronics. All categories of this research are quite novel and have never been duplicated by any other research facility.

### 1.3 Arrangement of Dissertation

This document is divided into ten chapters beginning with this introduction.

Table 1-1 summarizes the basic content of each chapter.

**Table 1-1.** Arrangement of dissertation with description of chapter content.

1	Introduction and Overview of Dissertation
2	Overview of Typical MEMS and CMOS Microtechnology
3	Overview of the Flip-Chip Assembly Process
4	Experimental Setup and Testing Procedures
5	Characteristic Modeling of Typical Flip-Chip Devices
6	Study of Flip-Chip Assembly onto Ceramic Substrates
7	Study of Flip-Chip Assembly onto Submount Modules
8	Study of Flip-Chip Assembly onto CMOS Electronics
9	Overview of Broad Design Concepts
10	Summary of Dissertation and Future Research

The first three chapters describe the dissertation and the general technology used to complete the research within it. A general overview of both MEMS and CMOS technology is provided as a review before the introduction and overview of flip-chip assembly is presented. An entire chapter is reserved for descriptions of flip-chip bonding equipment and special procedures used to design, fabricate and test flip-chip structures. Another chapter is devoted to the detailed modeling of the flip-chip devices developed as part of this research. Because this research spans a wide variety

of applications and types of flip-chip assembly, this chapter contains a broad description of the tools necessary to develop models of flip-chip devices.

Beginning with Chapter 6, the results of flip-chip assembly on ceramic substrates, submount modules, and CMOS electronics are each presented in separate chapters. Each category represents specific objectives and technical concerns that are sometimes unique to its intended applications. After each category of flip-chip assembly results, a summary of broad design concepts and future development is presented in which specific features are described which are applicable to multiple flip-chip assembly techniques. Likewise, the last chapter summarizes the achievements of the research and suggests future work for continuing this project.

## **CHAPTER 2**

### **OVERVIEW OF MICROTECHNOLOGY**

Although the field of MEMS was uniquely enabled by leveraging the integrated circuit industry, the methods by which MEMS are fabricated have expanded well beyond the standard photolithographic means by which integrated electronic devices are created. Additionally, micromechanical devices are highly application specific and often require specialized fabrication techniques in order to achieve some desired performance. As a result, the number of techniques that are available to create MEMS will continue to increase as long as new and more demanding applications are developed.

Currently, there are literally dozens of techniques for creating micromechanical structures such as wafer bonding, implantation etching, stereo x-ray lathing, and LIGA processing. Wafer bonding creates larger devices by fusing patterned wafers together to form features such as the large cavities and proof masses necessary for many accelerometers. Implantation etching uses ion implantation to selectively alter the doping concentration of bulk material in order to form desired shapes when the material is etched. Lathing uses a variety of high-energy beams to literally carve a block of bulk material into the desired structure. Finally, high-aspect ratio devices can be formed in the LIGA process which is a German acronym that

describes the technique of lithography, electroplating, and mold injection used to create devices that are many times taller than the minimum lateral feature size.

Although such a variety of fabrication techniques exist, surface micromachining of polycrystalline silicon (poly or polysilicon) remains the primary means by which designers create MEMS for a variety of growing applications. This process is described in some detail in the next section.

## 2.1 Introduction

Although microfabrication is often used to refer to any technique that produces miniaturized objects, it is important to note the scale on which the devices in the following chapters are created. To avoid any confusion with the scale of devices known as nanotechnology, the microtechnology presented in this chapter deals with objects that are measured in micrometers (microns) in which features and spacing between them are designed with increments of 1  $\mu\text{m}$  or more.

### 2.1.1 Definitions

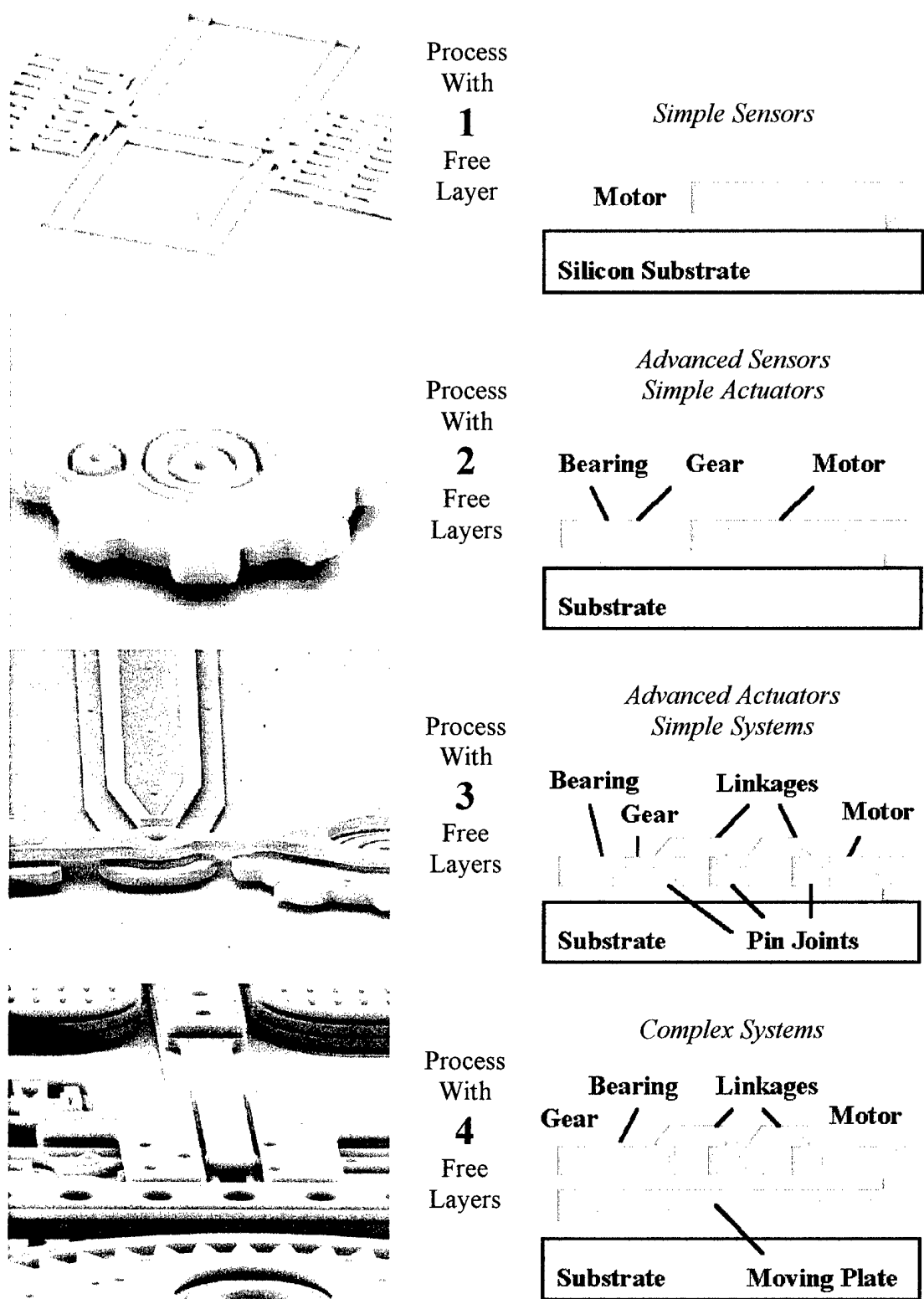
For this research, a “*module*” is the smallest substrate cell intended for flip-chip bonding. For instance, a “*host*” module contains all the upper layers of a device or array of devices intended for transfer to another “*receiving*” module designed to hold those features after they are released. Most host modules are diced portions of MUMPS chips that contain only the features to be bonded. The receiving module is usually another MUMPS substrate, ceramic substrate, or CMOS chip.

## 2.2 Introduction to Surface-Micromachining

The most commonly employed commercial foundries use the process of surface micromachining to create structures patterned in thin layers of polysilicon atop a single crystal silicon substrate. The substrate, identical to those used to create electronics chips, is first covered with a thin film of silicon dioxide and/or silicon nitride as an isolation layer. Then, alternating films of structural and sacrificial material are deposited over the isolation layer and patterned using standard photolithographic techniques. The number and thickness of layers and the mechanical properties of those layers are unique to each fabrication process.

Using some of the more common fabrication services, designers have typically been faced with a variety of problems and limitations which prevent the ideal optimization of devices. For instance, most processes have conservative design rules and minimum feature sizes which reduce the area of active surfaces or stretch the mechanical tolerances of joints and linkages. The conformal deposition of upper polysilicon layers over features patterned in underlying layers can create very adverse topographical effects which can either hinder or even prevent the operation of the device. Furthermore, these layers are typically plagued with high internal stresses which cause deformations or other undesirable mechanical behavior. Finally, and probably most significantly, the most common commercial services offer a maximum of only two releasable layers of structural material which dramatically limits the functionality of many devices. Figure 2-1 illustrates the relationship between the number of releasable or “free” layers and the resulting device complexity.





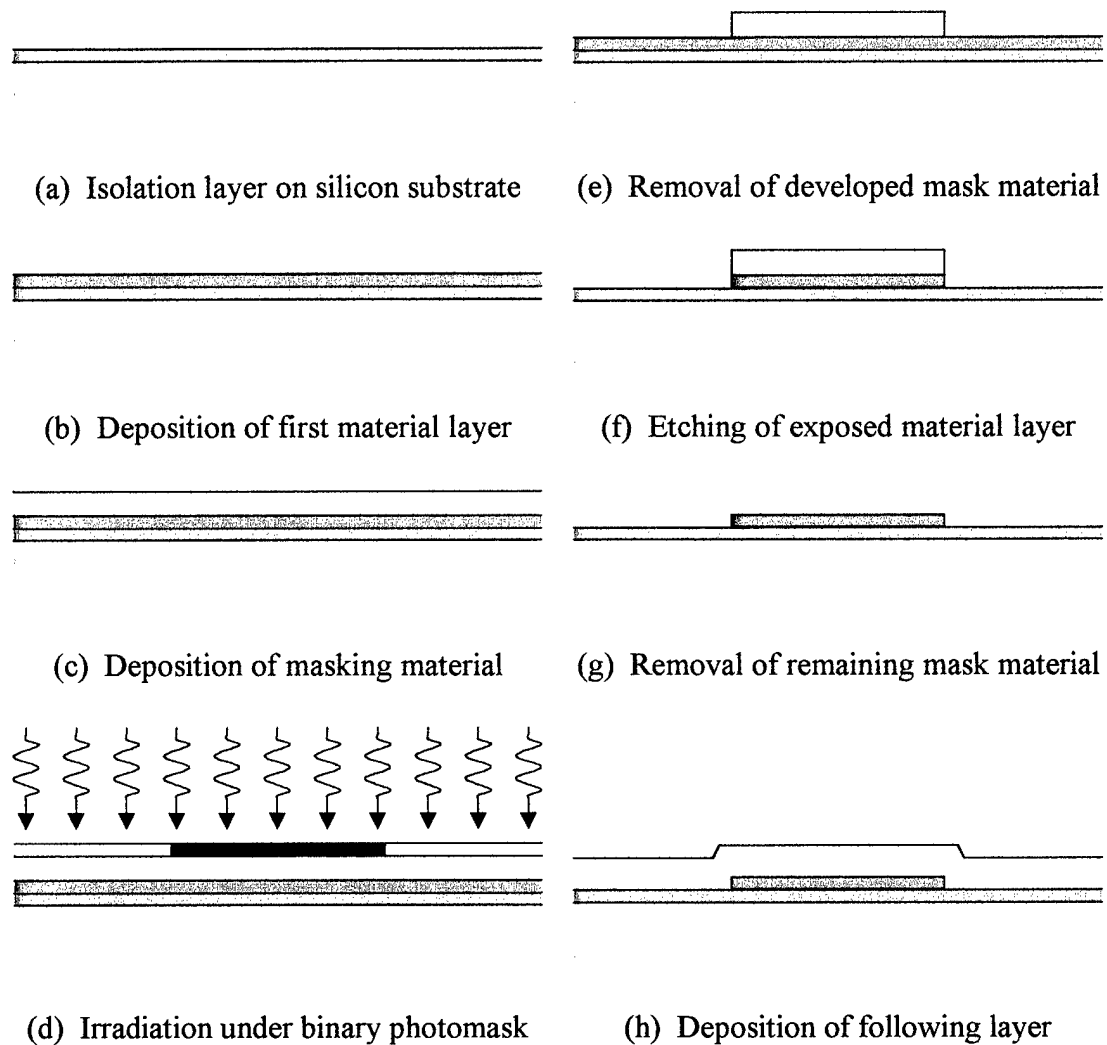
**Figure 2-1.** Illustration of device complexity by number of structural layers [2].

Probably the most widely used commercial fabrication service is known as the Multi-user MEMS Process (MUMPs) which is available from Cronos Integrated Microsystems. This process, initially developed by the Microelectronics Center of North Carolina (MCNC), offers only two releasable polysilicon layers with no special features or optimization. Although it is commonly used to create low-cost prototypes, more advanced fabrication services must be employed if more complex MEMS are to be realized. One advanced service growing in popularity is the Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT) process which now offers four releasable layers and a variety of optimized features such as rotating pin joints, planarization of structural layers, ultra-low stress polysilicon and reduced feature sizes and spacing. These services are discussed in greater detail in the following sections.

In addition to the releasable layers represented in Figure 2-1, most processes contain a ground structural layer that is patterned directly atop an isolation layer on the substrate and is therefore not releasable. Although not available to form movable structures, it is typically used for wiring or electrical shielding purposes which allows upper structural layers to be devoted to more critical features.

### **2.2.1 Introduction to Photolithography**

As previously described, the MEMS industry leveraged the majority of the fabrication technology from the IC industry. At the heart of that technology is the ability to deposit and pattern thin films of material on substrate surfaces. The use of photolithography to pattern these layers of material is shown in Figure 2-2 in which an arbitrary layer of material is deposited and patterned atop a silicon substrate.



**Figure 2-2.** Sequential cross section illustration of photolithographic processing.

The process starts with a silicon substrate shown in Figure 2-2(a) on which an isolation layer has been deposited. The material layer shown in Figure 2-2(b) is deposited on the entire surface of the substrate and a layer of masking material shown in Figure 2-2(c) is deposited immediately following. As shown in Figure 2-2(d), a binary photomask containing the desired layer pattern is placed over the surface of the masking material at which point the wafer is exposed to ultraviolet (UV) light.

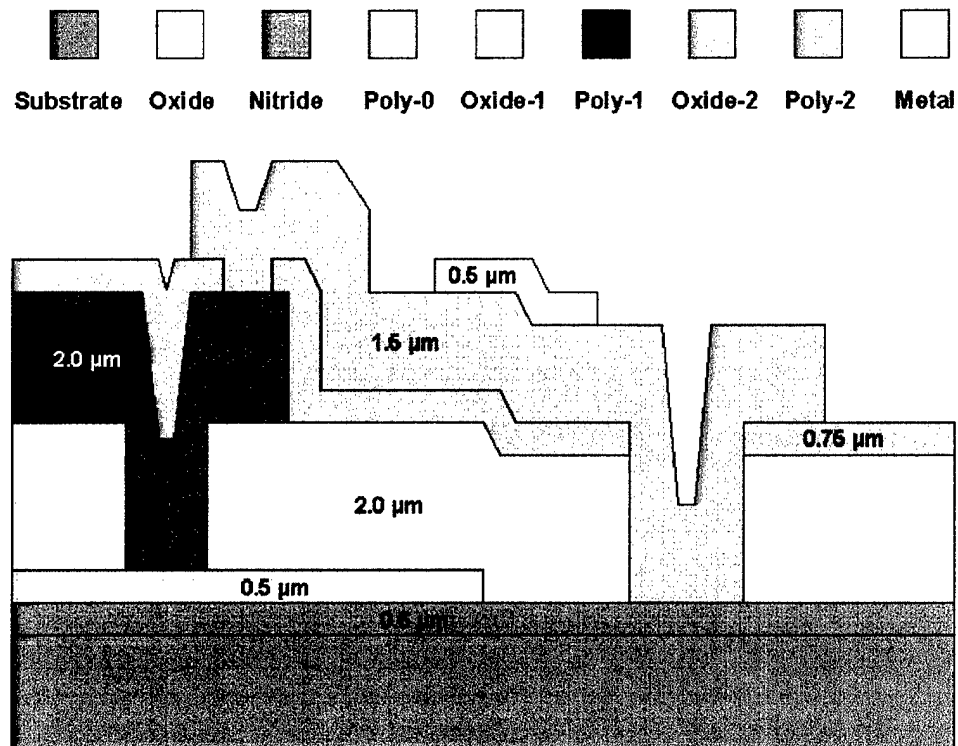
After developing the masking material, as shown in Figure 2-2(e), the excess portions can be selectively removed. As shown in Figure 2-2(f), the now exposed material layer is selectively etched to assume the shape of the desired layer pattern. Finally, as shown in Figure 2-2(g), the remaining masking material is removed from the substrate which leaves the original material layer in the desired shape. To build additional layers, the process is repeated whereby another material layer is deposited across the entire surface of the substrate. This new layer shown in Figure 2-2(h) is formed in a different material than the first such that alternating layers of structural and sacrificial material are used to form the desired mechanism.

The masking material, known as photoresist, is similar to the substance that coats standard camera film. As the fundamental element of photolithographic processing, it is photo-sensitive such that the material composition changes when exposed to specific wavelengths of light. For positive photoresist, the portion of the material that is exposed to light is removed. As shown in Figure 2-2(e), only the portion of the photoresist that was protected from the light under the photomask remains. The inverse is true for negative photoresist materials where only the exposed material remains. Depending on the complexity of the layer pattern, one type of material may be extremely more advantageous to use than the other.

Of particular interest in Figure 2-2(h) is the topography shown in the layer following the first patterned layer. All upper layers deposited onto patterned features of lower layers will assume their general shape and will therefore propagate often complex, irregular, and usually unwanted topography. Some foundry services offer a somewhat complicated planarization process to overcome such deformities.

### 2.2.2 Multi-User MEMS Process (MUMPS)

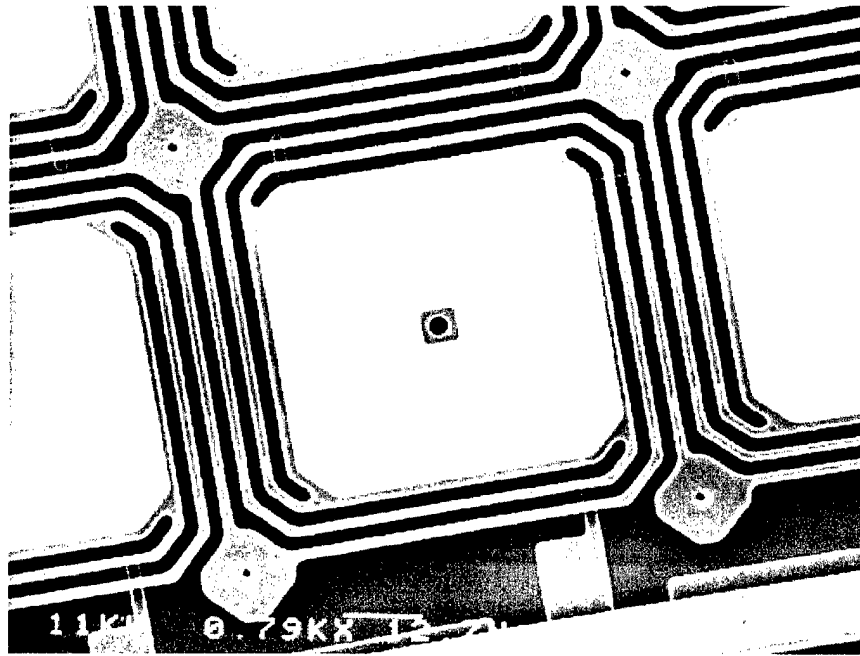
Most MEMS engineers are very familiar with the MUMPS process offered by Cronos Integrated Microsystems. It has been the affordable means by which countless government, industry, and university laboratories have fabricated devices for many years. Figure 2-3 illustrates the three structural layers of this process with the thin layer of gold that is deposited on the upper polysilicon layer.



**Figure 2-3.** Cross section illustration of the MUMPs fabrication process [after 3].

As evident in Figure 2-3, this process does not offer planarization such that the upper structural layers of the process conform to the features patterned in the layers beneath them. Unfortunately, this creates numerous problems for a variety of

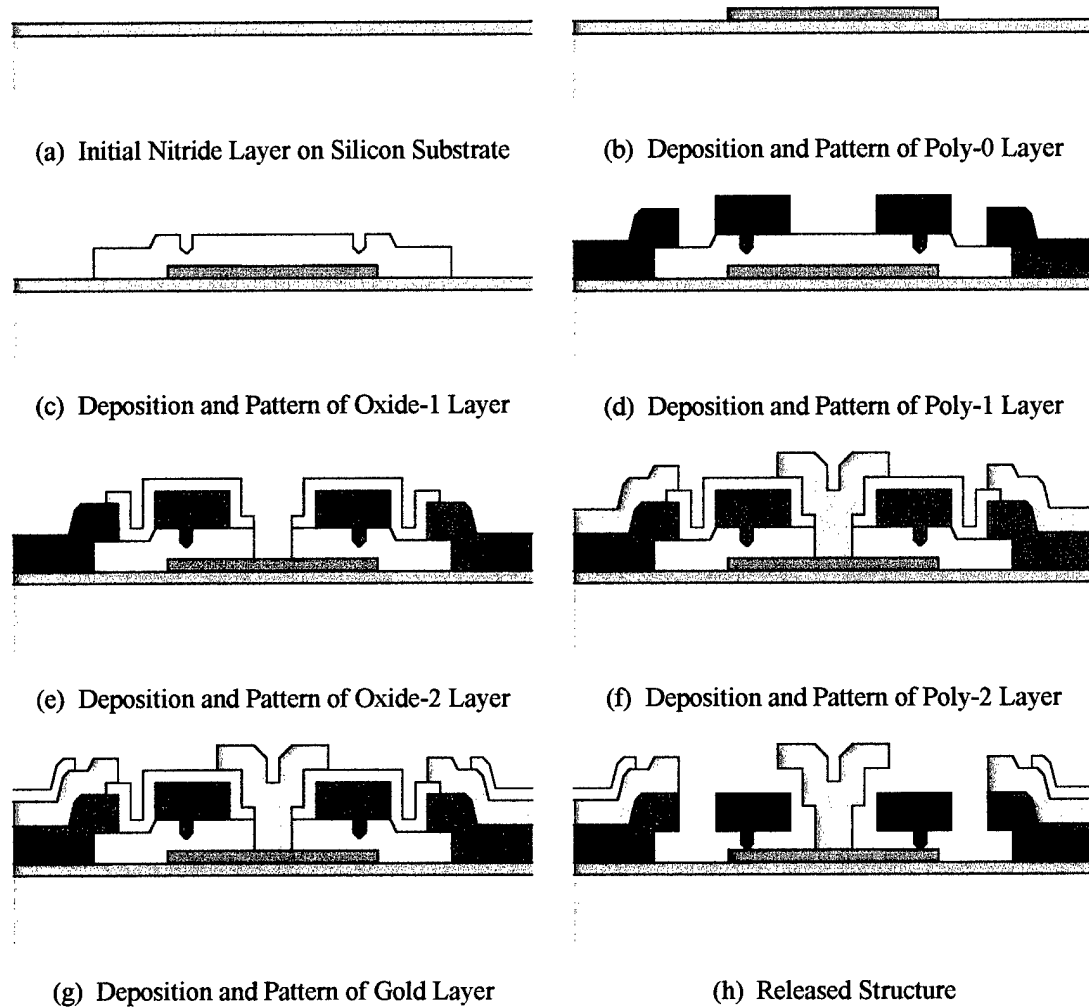
devices such as micromirrors which require flat reflective surfaces. For instance, the piston style micromirror device in Figure 2-4 illustrates some of the drawbacks to this fabrication process [4].



**Figure 2-4.** Micrograph of a micromirror device created in the MUMPs process.

The device shown in Figure 2-4 has bulky flexures surrounding each mirror surface which reduces the active surface area of the array. Since the process does not include planarization, these flexures would have created severe topographical effects in the mirror surface had they been placed beneath it. Additionally, the structural layers of the MUMPs process typically demonstrate moderate internal stress such that very large features tend to deform slightly. Finally, this process can produce feature sizes and spaces of no less than  $2\text{ }\mu\text{m}$  which creates additional problems for devices such as gears or hinges which require tight mechanical tolerances. Using the MUMPs

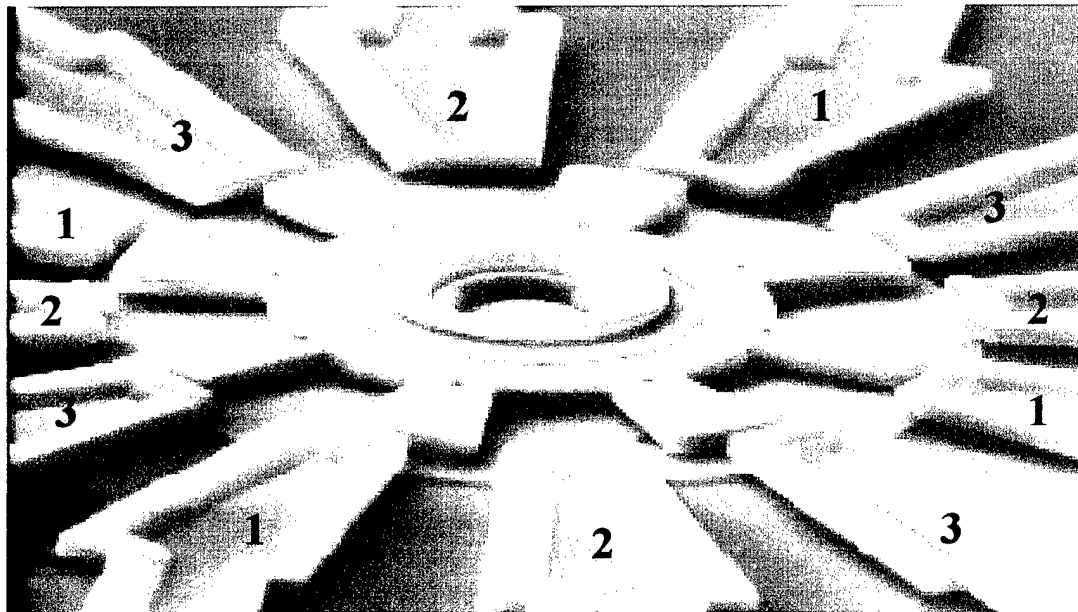
fabrication process, Figure 2-5 illustrates the sequential fabrication of a micromotor viewed through a cross section at the hub of the rotating gear. The color key shown in Figure 2-3 can be used to identify each of the layers.



**Figure 2-5.** Sequential cross-section illustration of micromotor fabrication [after 3].

The substrate shown in Figure 2-5(a) is covered with a layer of nitride upon which Figure 2-5(b) shows the ground Poly-0 layer patterned into a bearing plate. Figure 2-5(c) shows the Oxide-1 layer patterned with dimples to minimize wear from

repeated rotation. Figure 2-5(d) shows the Poly-1 layer patterned in the form of the gear and surrounding electrostatic actuators that will drive the motor. Figure 2-5(e) shows the Oxide-2 layer that isolates the gear along with the anchor cut that will connect the hub to the substrate. Figure 2-5(f) shows the Poly-2 layer that forms the hub and actuators and Figure 2-5(g) shows the metal layer that reduces resistance of the wires. As shown in Figure 2-5(h), the devices are released in a hydrofluoric (HF) acid etch that removes the sacrificial oxide layers to free the structural features. Figure 2-6 shows a micrograph of the resulting device.



**Figure 2-6.** Micrograph of resulting gear surrounded by electrostatic actuators [3].

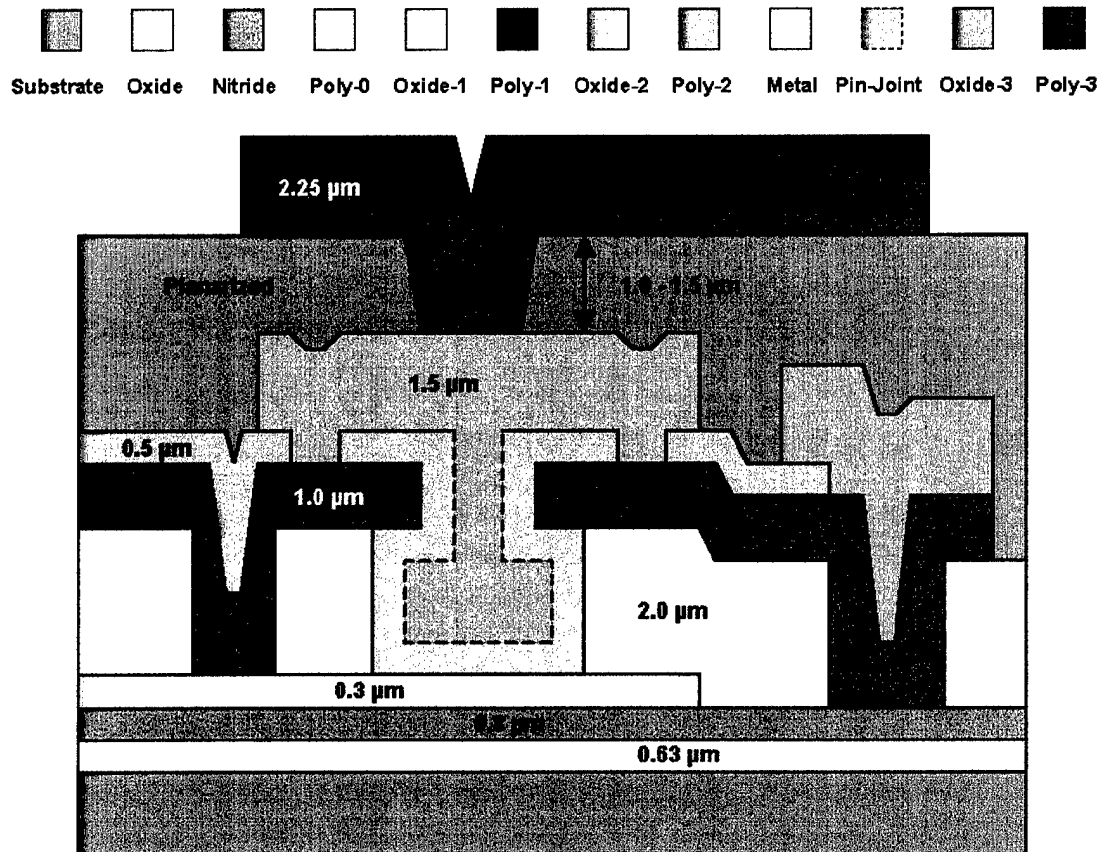
Four sets of three electrostatic actuators are charged in sequence to lead the nearest tooth of the gear to produce rotation about the hub at the center of the device. The gold layer illustrated in Figure 2-5(g) is not shown.



### 2.2.3 Sandia Ultra-planar Multilevel MEMS Technology (SUMMiT)

As previously described, the complexity and quality of micromechanical devices is directly related to the capabilities of the fabrication process in which it is created. The SUMMiT process offered by Sandia National Laboratories is one of the best in the world. It is similar to the MUMPS process with some notable exceptions.

Figure 2-7 illustrates many of the features of this process.



**Figure 2-7.** Cross-section illustration of the SUMMiT fabrication process.

First, as illustrated in Figure 2-7, this process has a fourth structural layer that is planarized to remove topographical effects caused by the deposition of thin films

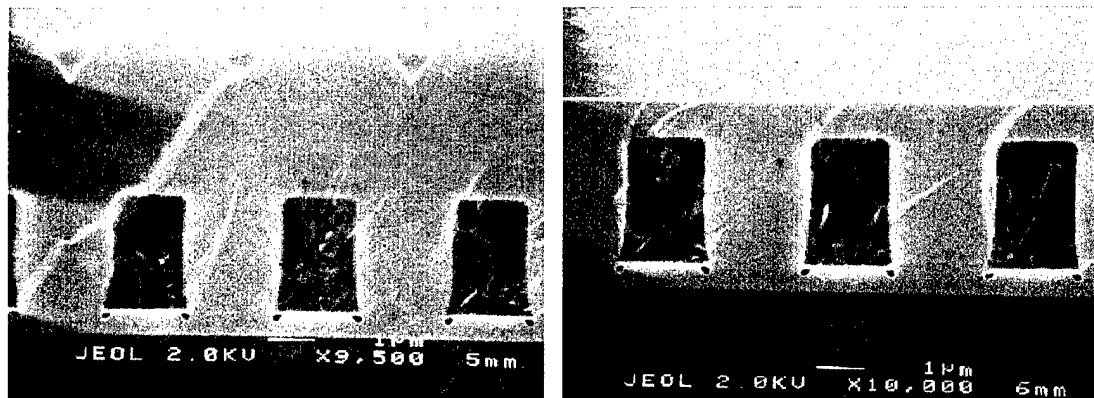
over features patterned in underlying layers. This advanced process makes highly complex and intricate micromechanical systems easily realizable. This SUMMiT IV technology has recently been expanded to SUMMiT V in which another planarized layer has been added to the process.

Additionally, the SUMMiT process offers other unique advantages which include ultra-low-stress material, design rules and features of only 1  $\mu\text{m}$  with 0.1  $\mu\text{m}$  mask resolution, and the ability to make flanged gear hubs with a “pin joint” cut. This same joint can also be used to create a variety of novel mechanical locking mechanisms in place of flexures or other rigid support structures.

Furthermore, the deposition of ultra-low-stress polysilicon developed by Sandia enables SUMMiT designers to use larger expanses of structural material without concern that the device will curl due to internal stress. The reduced feature sizes further increase active surface areas and device density while the mask resolution allows for very precise and consistent flexure fabrication which would typically be a problem when features drawn at angles to the mask axes are snapped to larger mask grids in a disfiguring step pattern.

Finally, the uppermost sacrificial oxide is planarized using Chemical Mechanical Polishing (CMP) so that the following structural layer (Poly-3) is flat [2]. This layer has the potential to eliminate all unwanted mirror surface topography which is normally induced by its conformal deposition over the mechanical features of the underlying layers. Initial SUMMiT test devices demonstrate a small degree of print-through topography in which not all of the conformal effects of the layer were removed. This effect was observed in first-generation micromirror devices [5].

The devices are CMP planarized by placing the entire wafer face down in a chemical slurry and slowly polishing the normal oxide deposition profile, shown in Figure 2-8(a), down to a smooth surface, shown in Figure 2-8(b). Without this process step, as can be seen in Figure 2-8(a), the following layer of polysilicon would conform to the oxide and result in a deformed surface which is not well suited to most optical applications or complex mechanical motion [2].



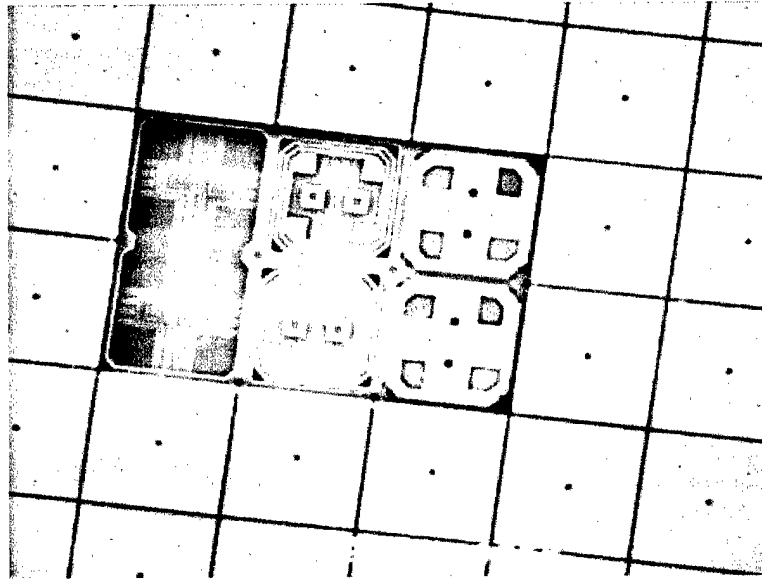
(a) Conformal Deposition Profile

(b) Planarized Deposition Profile

**Figure 2-8.** Illustration of CMP planarization of sacrificial oxide layers [2].

The first-generation micromirror devices which demonstrated the slight print-through topography were fabricated in the first two runs of the SUMMiT process. This process was originally designed for mechanical devices such as gears, motors, and inertial sensors in which the upper layer of the process (Poly-3) was planarized to prevent trapping or hindering these devices with topographical effects in drive linkages and other interconnects. This planarization was designed for mechanical tolerances and performed by simply polishing peaks in the uppermost sacrificial oxide down to the same level as the lowest point of the layer [2]. Although this

procedure was never intended to planarize layers for optical devices, the quality of micromirror devices that can be achieved using additional structural layers of planarized material is far better than with MUMPS fabrication. Figure 2-9 shows a significantly higher quality device fabricated in the SUMMiT IV process.



**Figure 2-9.** Micrograph of a micromirror created in the SUMMiT process [2].

The device has fine features placed under the mirror surface resulting in a nearly ideal active surface area within the array. The mirror surface is planarized so that the features patterned in the layers beneath it do not adversely affect the optical behavior of the reflective surface. Finally, this optimized device shows complex wiring beneath elevated electrodes that enable large arrays of individually addressed devices. Fabrication of this device is only possible using additional structural layers which include a planarized upper layer. For the purpose of comparison, this is precisely the benefit and added capability of creating flip-chip micromirror arrays.

## **2.3 Introduction to CMOS Technology**

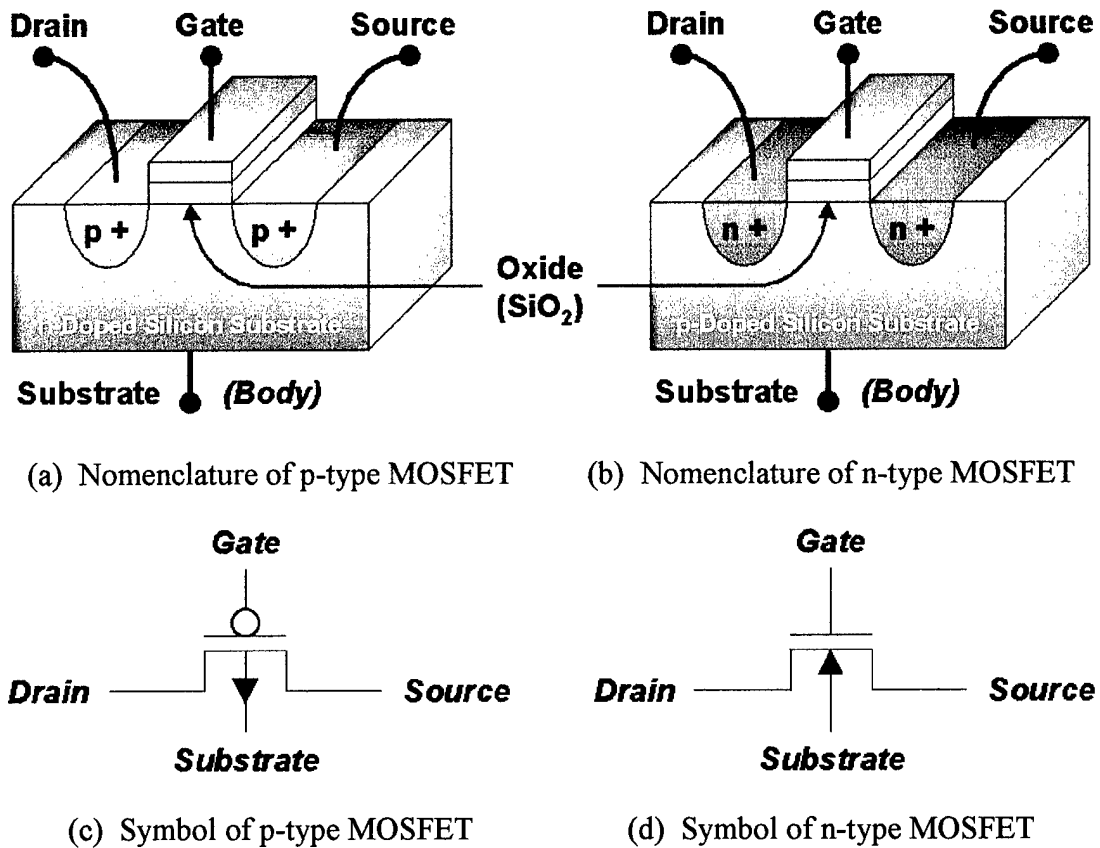
As previously mentioned, the techniques used to fabricate early MEMS were directly leveraged from the integrated circuit (IC) industry. Microelectronic chips are typically created by the deposition and patterning of various thin material layers between isolation oxide layers. In fact, a typical IC can be released in the same manner as a MEMS chip to free the features drawn in the structural layers. Unfortunately, the very thin, high stress layers that are typical among IC services are poorly suited to forming usable micromechanical structures.

Although there are numerous types of electronic technologies, each with distinct benefits suited to specific applications and devices, none is more common or widely used than Complementary Metal Oxide Semiconductor (CMOS) processing. This technology uses photolithography to pattern regions of doped silicon and surface layers to create both n-type and p-type MOS Field Effect Transistors (MOSFETs) on a single silicon chip. The two types of transistors are linked together in such a way that the inherent switching benefits of each is preserved so that their combined operation allows for fast, virtually fault-free digital processing.

### **2.3.1 Introduction to MOSFET Design and Operation**

The MOSFET devices consist of a source node and a drain node between which a gate node controls the flow of charge carriers within the channel beneath it. The gate typically consists of a thin line of polysilicon separated from the substrate by a thin oxide layer known as the gate oxide. Figure 2-10(a) illustrates the composition

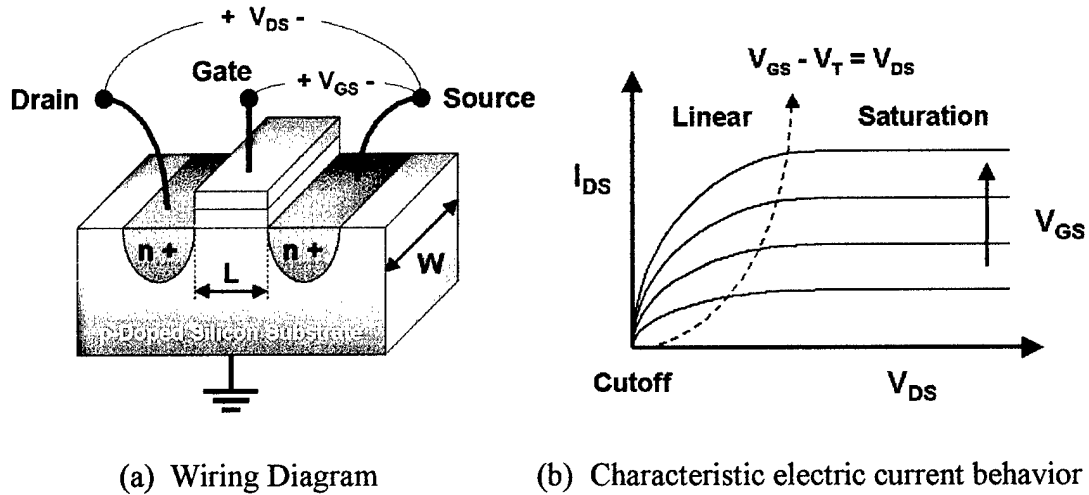
of a typical p-type MOSFET on a phosphorus doped (n-type) silicon substrate where twin wells of high concentration boron diffusion (p+) rest on both ends of the gate. Conversely, Figure 2-10(b) illustrates the composition of a typical n-type MOSFET where the well and substrate doping is reversed. Although the devices are symmetric about the gate, the source and drain nodes are so named as a wiring convention.



**Figure 2-10.** Illustration of MOSFET nomenclature and symbolic representation.

The symbolic diagrams for both devices are shown in Figure 2-10(c) and (d) which illustrate the substrate or “body” contacts that must be made in order to enable the devices. These symbols are used in schematic diagrams of complete circuits.

A wiring diagram for a typical n-type MOSFET is shown in Figure 2-11(a) in which the gate and drain potentials,  $V_{GS}$  and  $V_{DS}$ , respectively, are identified. The source nodes of n-type MOSFETs are typically connected to ground so that  $V_{DS}$  and  $V_{GS}$  represent the applied potentials at the drain and gate, respectively.

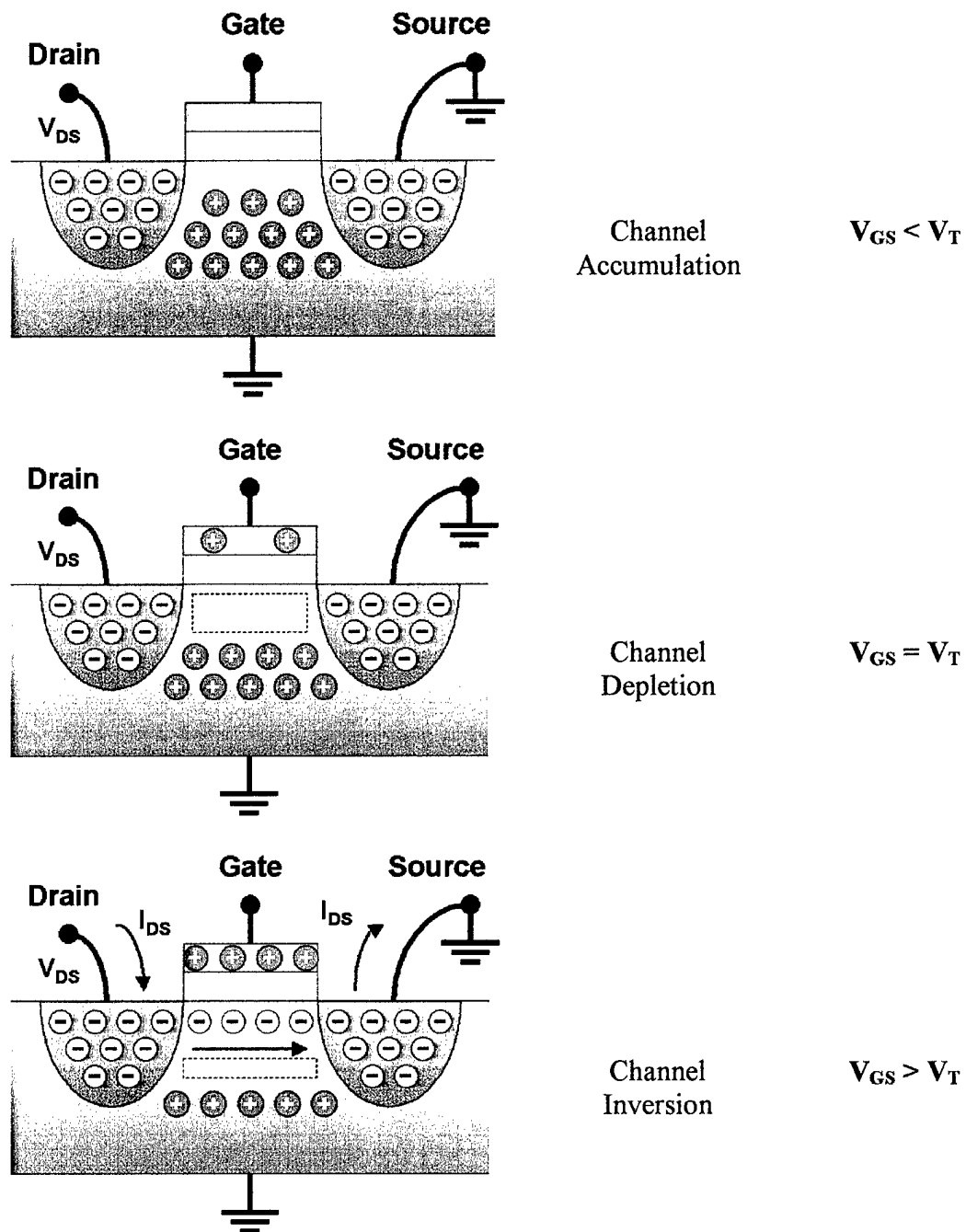


**Figure 2-11.** Wiring diagram and behavior curves of n-type MOSFET device.

The current that is allowed to flow through the device is a function of these applied potentials as well as a threshold voltage,  $V_T$ , that is inherent to all devices. As illustrated in Figure 2-11(b), the current flowing from the drain to the source,  $I_{DS}$ , increases as either the gate potential or the drain potential increase. For most devices, the drain potential is fixed and the gate potential is the trigger or input signal of the device. In this manner, the switching capabilities of the MOSFET are regulated by a single analog drive signal.

The behavior of the n-type MOSFET is better illustrated in Figure 2-12 in which the gate potential starts out below the threshold voltage and is then increased.

As illustrated in Figure 2-12, the device is originally switched off and no current passes through it. There is no electric field within the device to create a channel that would allow the charge carriers to pass through the device.



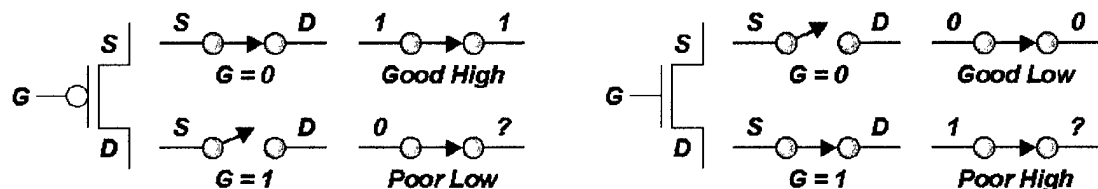
**Figure 2-12.** Illustration of n-type MOSFET state as a function of gate potential.



As the gate potential is increased, however, the induced electric field depletes the original channel of opposing charge carriers and eventually inverts the channel so that a current can pass through the device.

Although MOSFET devices are continuous in nature where various potentials can be applied to each node to obtain unique switching behavior, the devices are most commonly used in digital mode where only a ground (low) or supply (high) potential is induced on any node. For such operation, the digital value of 0 represents a low or  $V=0$  volt potential and a value of 1 represents a high or  $V=V_{dd}$  potential. The supply voltage,  $V_{dd}$ , is used to power the entire circuit and is typically 3-5 volts depending on the current state of technology. The perpetual trend toward lower power electronic devices continually reduces this potential.

The switching characteristics of the devices are quite unique. As shown in Figure 2-13(a), the p-type device is activated by a low potential on the gate and will typically pass a high signal with little loss. Unfortunately, the same device does not conduct a low signal well and will typically allow the drain to drift to some potential between the supply and ground.



(a) Switching of p-type MOSFET

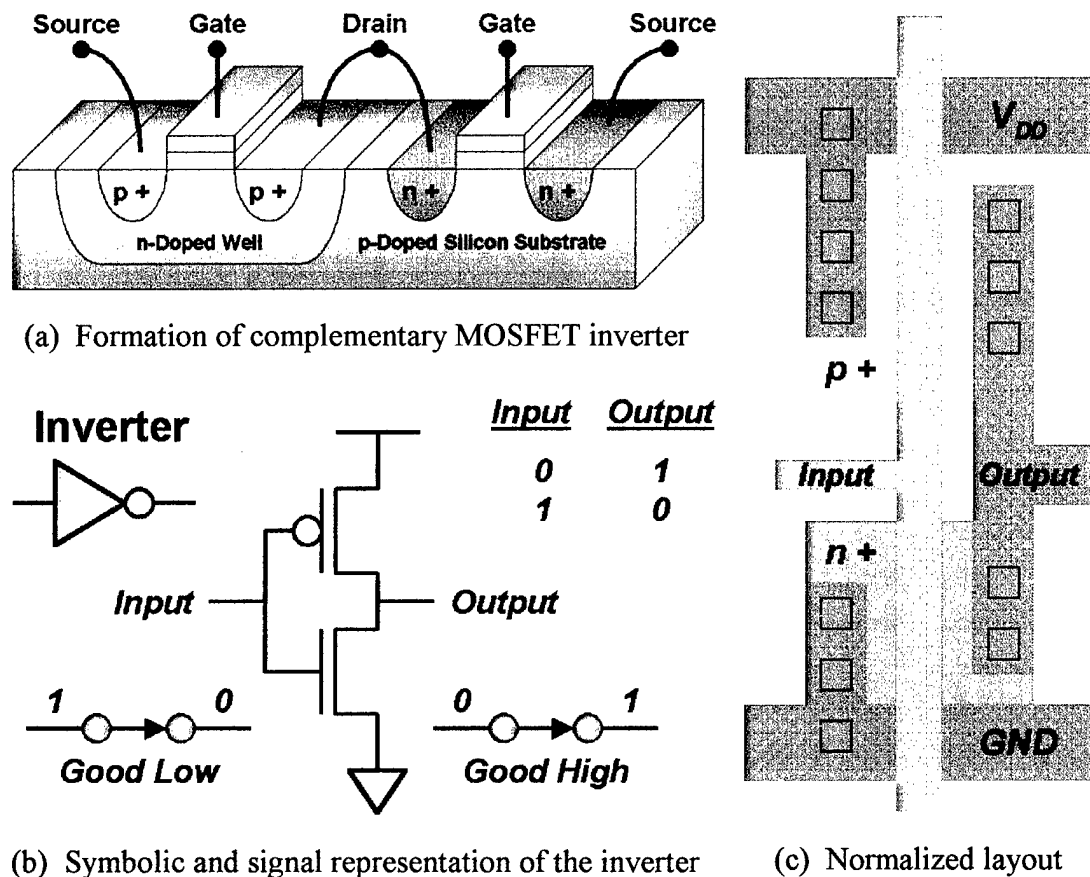
(b) Switching of n-type MOSFET

**Figure 2-13.** Illustration of p-type and n-type MOSFET switching characteristics.

Conversely, as shown in Figure 2-13 (b), the n-type device is activated by a high potential and passes a low signal with little loss. The same device does not conduct a high signal well and will pass a potential lower than the supply. When either device is not activated, the drain will float if not connected to another device or signal.

### 2.3.2 Introduction to Complementary MOSFET Structures

Since each device is not ideally suited to switching both signals, a complementary architecture is used in which each channel switches the best signal.

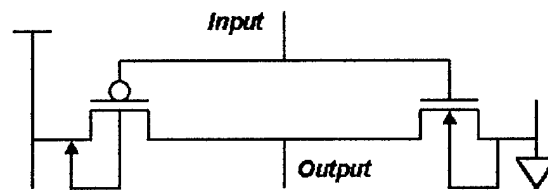


**Figure 2-14.** Formation of a complementary MOSFET inverter logic structure.

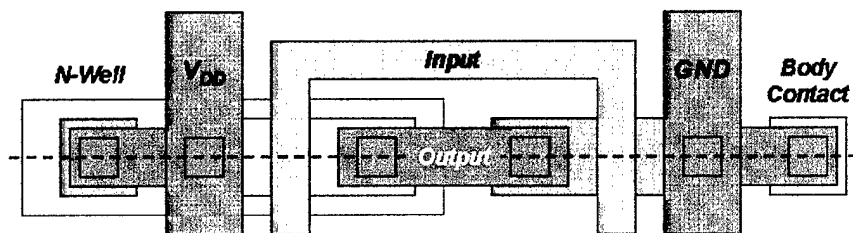
Figure 2-14 illustrates the simplest complementary MOSFET (CMOS) structure. This inverter produces the opposite signal on the output as placed on the input and passes either signal with little loss since the appropriate channel is used in either case.

### 2.3.3 Overview of CMOS Fabrication Process

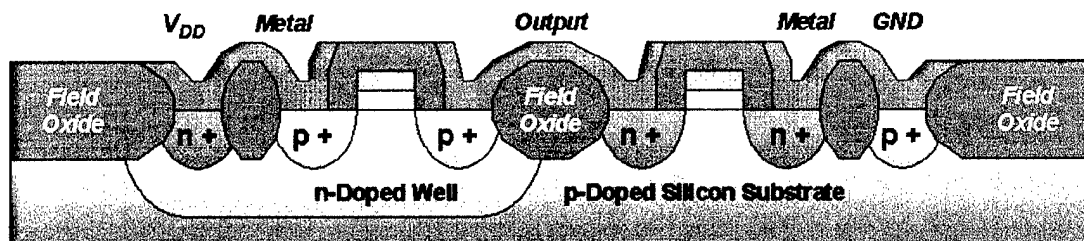
Any particular CMOS foundry service starts with either a boron doped (p-type) or phosphorous doped (n-type) silicon substrate. In order to form complementary devices, the opposite type of well must be diffused into the substrate.



(a) Schematic view of a typical CMOS inverter



(b) Overhead layout view of a typical n-well CMOS inverter



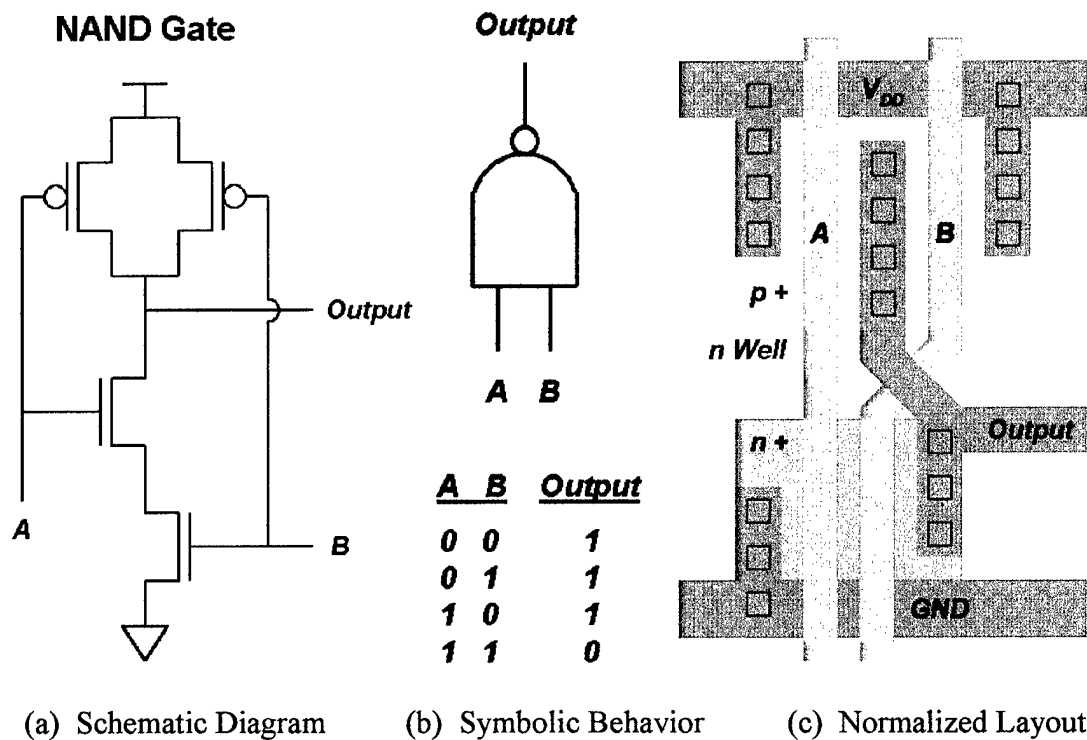
(c) Resulting cross section view of a typical n-well CMOS inverter.

**Figure 2-15.** Illustration of a typical n-well CMOS inverter showing critical features.

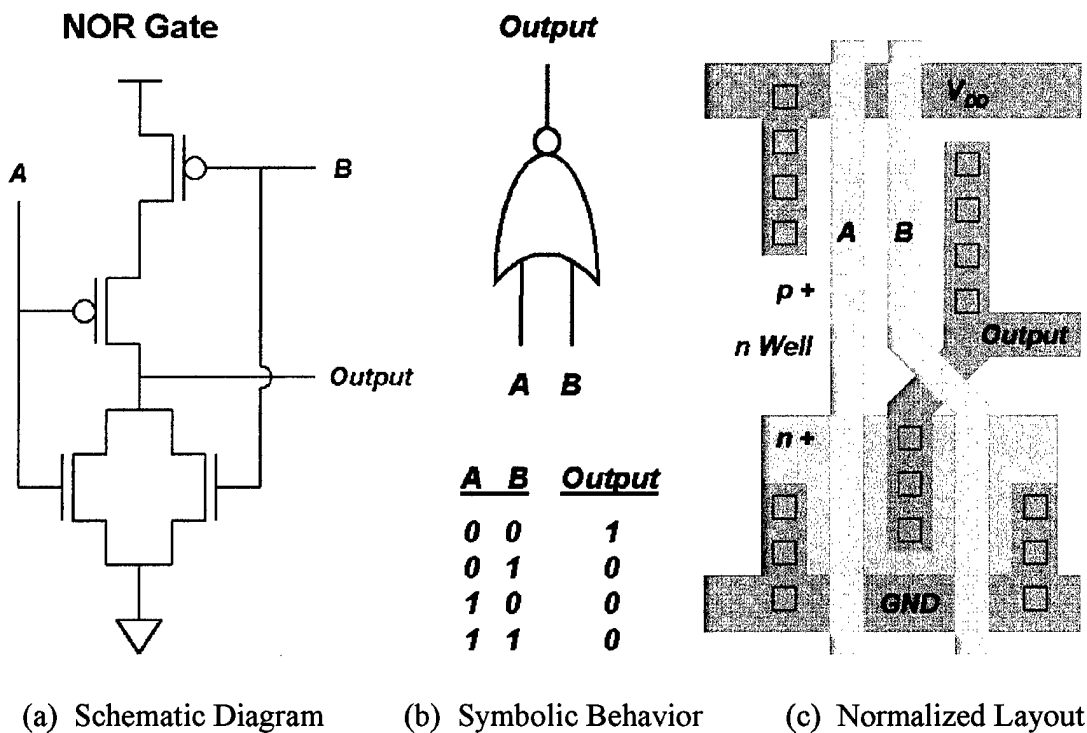
As illustrated in Figure 2-15, the n-well shown in Figure 2-14(a) must be drawn around any p-type transistor such that the appropriate charge carriers are present. Figure 2-15(b) illustrates a typical cross section of the inverter as it would be fabricated in most CMOS services. It consists of several doped regions beneath the original surface of the substrate and several layers of metal and polysilicon above it. These layers are patterned by the same photolithographic process that is used to create MEMS in surface micromachining services. The result is the cross section shown in Figure 2-15(c) which is more recognizable as the original MOSFET devices forming the inverter illustrated in the previous section.

Due to the inverting nature of complementary architectures, the principle gate structures that form the unit cells of digital logic generate output signals that are inverted functions of the input signals. The inverter is the simplest of these structures and simply returns the opposite of the digital signal that is present on the input. The remaining principal structures are “Not AND” (NAND) and “Not OR” (NOR) gates which process two input signals. These three logic structures form the fundamental basis from which highly complex digital processing functions can be formed.

For instance, the Exclusive OR gate (XOR) is often used to compare two signals to identify whether they are the same. Since either signal could be either high or low, the process by which they are compared is somewhat more complicated than simply using an inverter or one of the other gates. The three gates that form the digital logic basis are connected together in such a manner as to obtain an output that is high if only one of either input signal is high, but not both. By adding an inverter to the end of this gate, the output is high only when the input signals are the same.



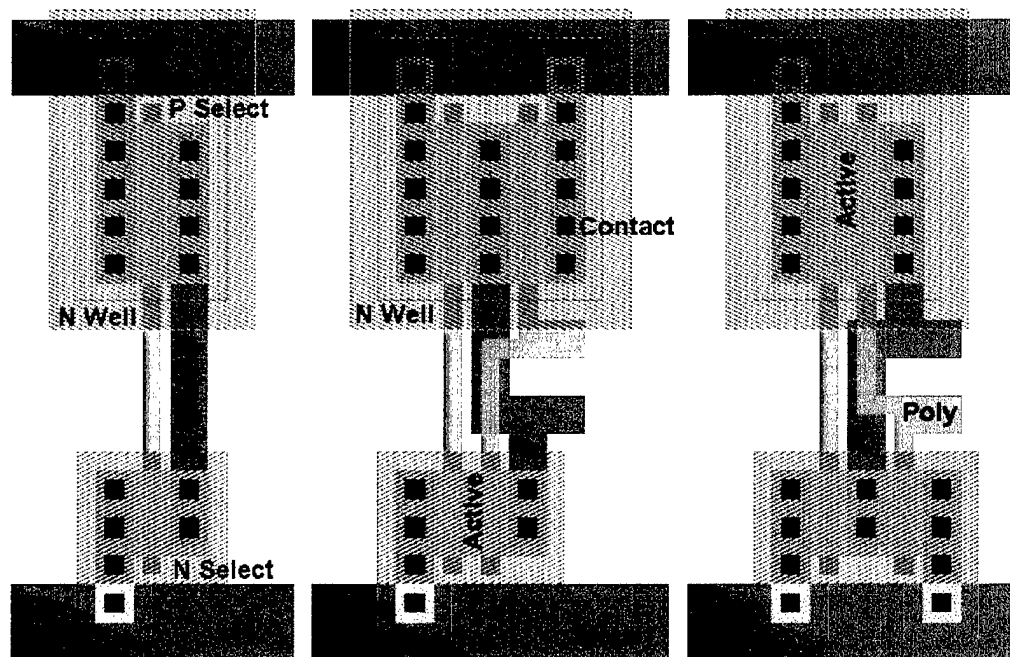
**Figure 2-16.** Formation of a typical CMOS NAND (Not AND) logic structure.



**Figure 2-17.** Formation of a typical CMOS NOR (Not OR) logic structure.

The representation of the NAND and NOR gates are somewhat similar to the inverter. As illustrated in Figure 2-16 and Figure 2-17, respectively, the same complementary architecture is employed to produce the desired output. Only the manner in which each MOSFET is connected changes the output of the particular logic structure. The AND and OR functions can be generated by simply adding an inverter to the end of the corresponding principal gate structure.

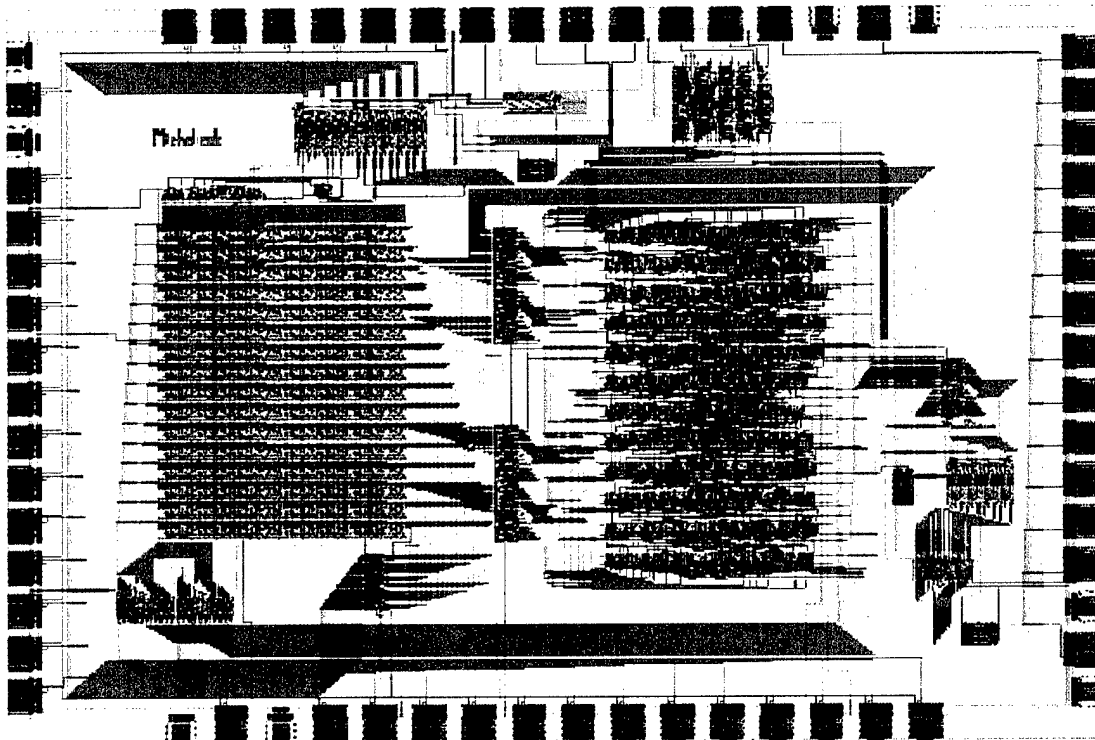
Using these basis structures, a set of standard cells can be defined such that the same gate layout can be scaled and inserted into different CMOS layouts. One of the primary benefits of this approach is that standard cells do not change as CMOS technology advances to smaller and smaller features. Figure 2-18 illustrates these standard cells in which one of each of the basis gates is defined in layout form.



(a) Standard Inverter      (b) Standard NAND Gate      (c) Standard NOR Gate

**Figure 2-18.** Illustration of the minimum set of standardized logic structure cells.

When designed with input and output bond pads, large numbers of these structures form a working CMOS chip that can be designed to perform any customized task such as numerical calculations, system monitoring, threshold detection, or timing functions to name only a few applications. Figure 2-19 shows a layout of a Reduced Instruction Set Computer (RISC) processor.



**Figure 2-19.** Layout of a microprocessor fabricated in a standard CMOS foundry.

This processor performs the same type of calculations as the processor in a standard desktop computer. Each component within the layout is comprised of complementary transistors that act in the same manner as the inverter to selectively transmit digital data between components and finally to the output pads.

### **2.3.4 Introduction to the MOSIS Service**

Customized CMOS chips can be fabricated by any number of commercial foundries throughout the world. Each foundry has a distinct set of design rules and special features that are offered to designers as capabilities of the service. In the United States, however, there is a single organization that acts as a user interface to the majority of foundries offering such services. This organization, known as MOSIS, maintains a database of currently available fabrication services and the technical and administrative details required to submit designs for fabrication. Engineers simply select the process of choice and download the technical information such as the size of the chip, the available layers, and any standard cell libraries that may be offered. Once the chip is designed, it is simply uploaded to MOSIS by the due date and the chip is sent to fabrication. Because of the highly volatile and forever advancing electronics industry, it is highly unlikely that any single CMOS designer could maintain an expertise in more than a single fabrication process without the critical MOSIS service.

## **2.4 Integrated Microsystems**

One of the most valuable developments in MEMS is the ability to integrate micromechanical devices with control electronics. It has been nearly impossible to fabricate both on the same chip due to incompatibilities in temperature and sacrificial layer material. Therefore, less ideal means of integration have been used. First, the assembly of Multi-Chip Modules (MCMs) has been widely used to connect the input

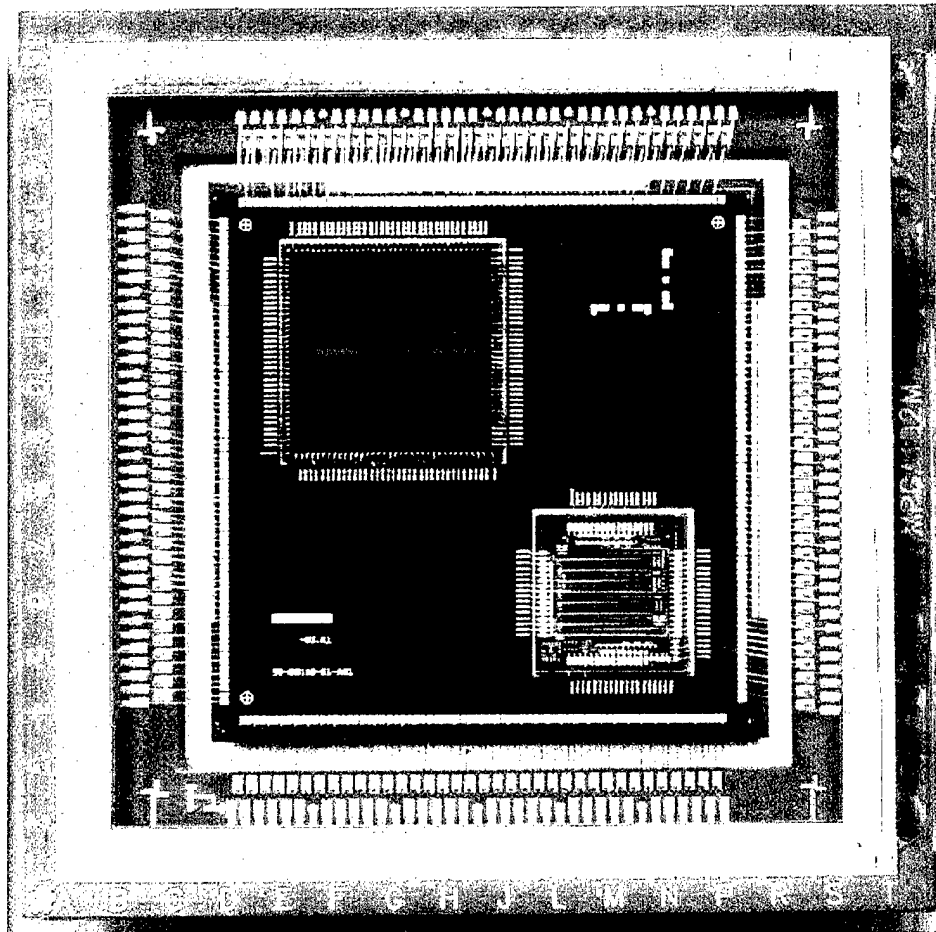


and output devices of electronics chips to those of the MEMS chips. Second, flip-chip bonding of CMOS electronics onto MEMS substrates has been widely used as a means to minimize wiring traces and increase wiring density. Finally, the recently developed Integrated MEMS (IMEMS) “trench prefabrication” technique allows simple devices to be fabricated beneath the surface of a CMOS wafer with a few extra preprocessing steps.

#### **2.4.1 Multi-Chip Modules (MCM)**

A number of commercial services specialize in producing MCMs which combine control electronics with various MEMS sensors or other off-chip components. The module sets each component on a single substrate and typically overlays the contacts with a High Density Interconnect (HDI) pattern that connects the input and output pads of the individual chips to those of the others. As a result, the total number of address lines required for input and output signals to the entire microsystem are significantly reduced.

It should be noted, however, that this approach is only an improvement in the wiring between chips. It does not increase the performance of the MEMS nor does it enable new devices or allow the removal of unwanted processing materials. This type of integration is not well suited to specific applications that require these enhanced features. Figure 2-20 illustrates a typical MCM showing the individual chips within.

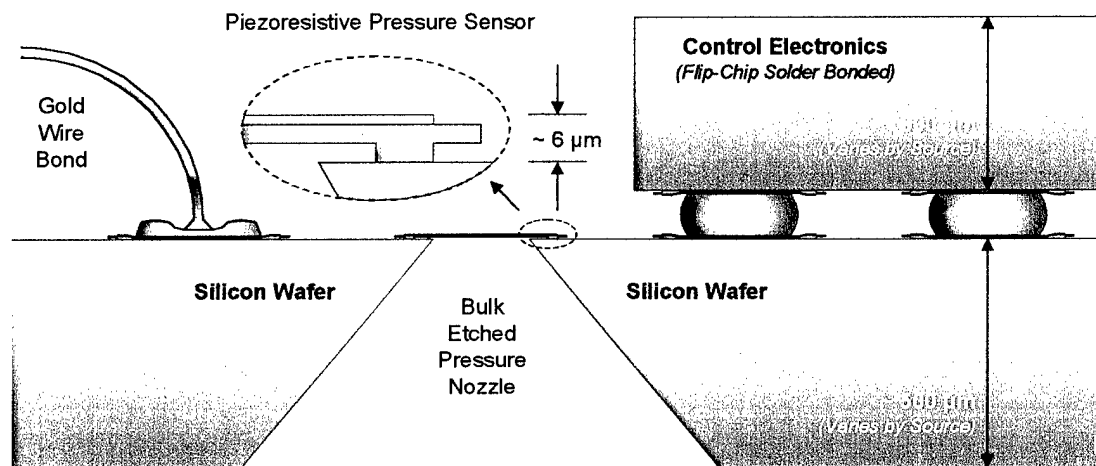


**Figure 2-20.** Photograph of a typical MCM enabling microsystem integration [6].

This microsystem shows individual chips each with a set of contacts that must be wired to other chips within the module or wired to the input or output pads of the microsystem. Normally, each of these traces must be wired between chips on a much larger packaging scale, but the use of HDI within the module means that many of them are ignored by the interface to the module. Therefore, address complexity can be reduced while improving processing capabilities such as increased speed and reduced power consumption.

### 2.4.2 Flip-Chip Bonding

Another common means of microsystem integration is flip-chip bonding in which a control electronics chip is inverted and bonded onto another substrate or work surface. As with MCM integration, such an approach is purely a wiring convenience that increases performance of the entire system. Flip-chip bonding does not improve material selection nor does it enable more functional or highly complex surface micromachined components. Figure 2-21 illustrates a typical example of flip-chip bonding in which a piezoresistive pressure sensor requires control electronics to analyze the current passing through the sensor.

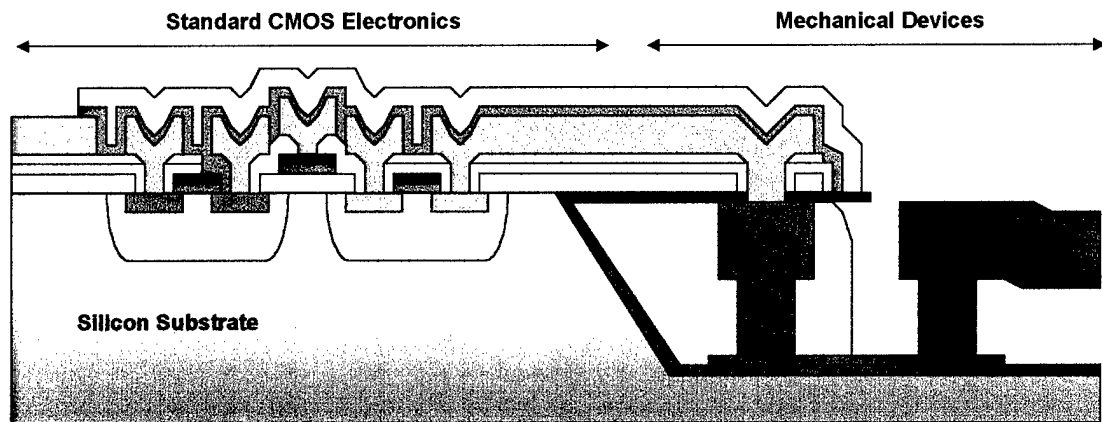


**Figure 2-21.** Illustration of an integrated microsystem flip-chip bonding application.

Again, many commercial foundries exist which can produce such systems, but they merely combine two standard commercially fabricated chips. Therefore, no increased performance of each individual chip can be realized using this form of flip-chip bonding nor is a fundamentally new technology enabled.

### 2.4.3 Trench Prefabrication Integrated MEMS (IMEMS)

One of the most interesting approaches to microsystem integration of MEMS and CMOS electronics is the IMEMS approach developed by Sandia National Laboratories. Normally, the temperature at which MEMS are annealed to reduce residual stress is sufficiently high to destroy the doping profiles in the CMOS electronics that may already exist on the substrate. However, if the MEMS are created first, it is difficult to process the CMOS features with large structures erected above the surface of the substrate. The solution, shown in Figure 2-22, is to build the MEMS in a trench beneath the surface of the substrate and fill it in with oxide so that the surface of the substrate remains planar and ready for CMOS processing.



**Figure 2-22.** Illustration of IMEMS fabrication of integrated microsystems [7]

The MEMS consist of only one releasable layer and are encased in oxide that is planar to the surface of the substrate. Therefore, the CMOS portion of the wafer can be processed as though it is a bare silicon substrate. After completion, the CMOS area is masked off so that the release etch that frees the MEMS will not remove the

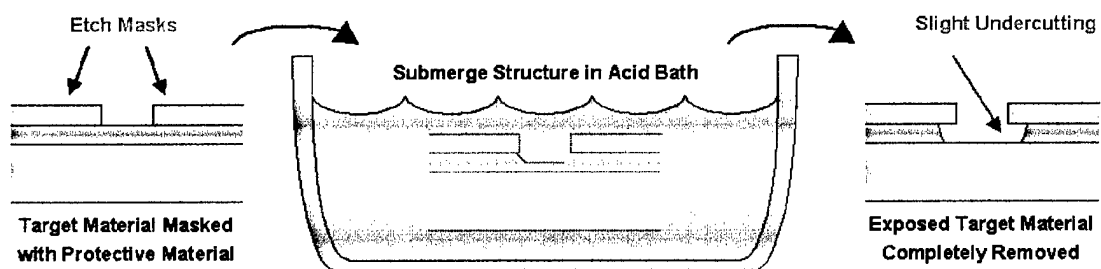
same oxide that is critical to the CMOS operation. Although it is a novel approach, it once again does not improve the MEMS performance nor enable advanced structures.

## 2.5 General Microfabrication Technology

This section contains basic descriptions of a few microfabrication techniques that are discussed in the following chapters. Some concepts are presented using the specific devices that are developed as part of this research.

### 2.5.1 Wet Etching

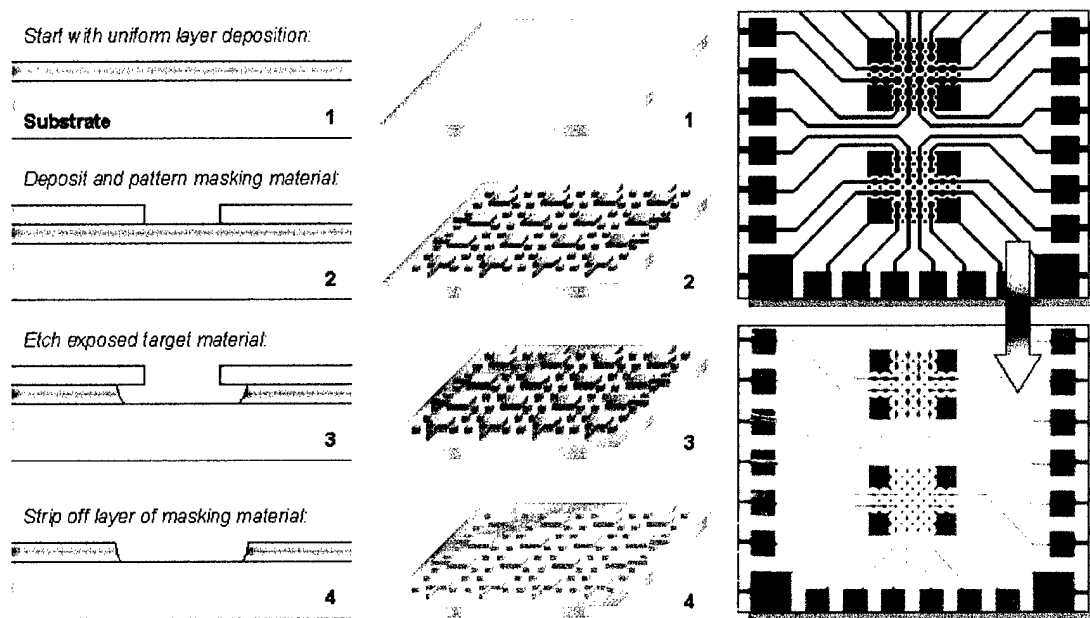
As illustrated in Figure 2-23, a layer of material can be photolithographically patterned to form an etch mask. This mask is used to protect another layer of material when it is submerged in an acid bath designed to etch the exposed material.



**Figure 2-23.** Illustration of wet etching to remove exposed target material.

When the test device is removed from the bath, only the exposed material beneath the mask has been removed. The mask material is then stripped using another bath.

This type of microfabrication will be employed to pattern gold features on the surface of ceramic receiving substrates intended for flip-chip bonding. As illustrated in Figure 2-23, a masking material is used to protect the portions of the material that are intended to remain on the substrate. Figure 2-24 illustrates the process by which address electrodes, address wires, and probe pads are patterned on the substrate.



**Figure 2-24.** Illustration of the use of wet etching to form gold wiring features.

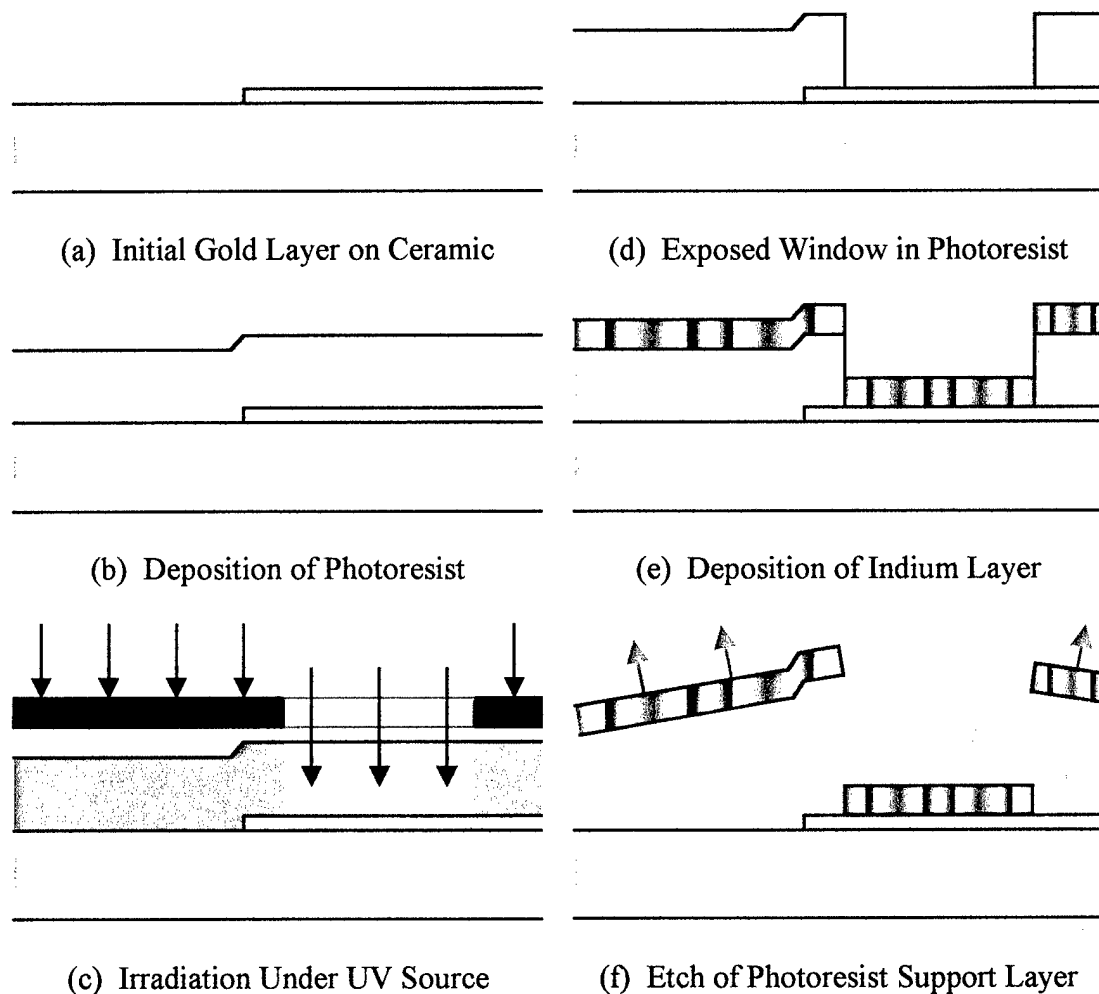
Once the gold is etched and the mask removed, the features that remain on the substrate are those drawn in the photomask used to pattern the masking material. This process is used to form ceramic substrates for flip-chip bonding of variable capacitors for Radio Frequency (RF) applications.

To fabricate such flip-chip devices, a layer of indium must then be deposited and patterned on the gold bond pads to secure the bond pads of the flip-chip structures. This material acts as an adhesion layer between them and must only be

placed where the two bond pads meet. Rather than forming this layer by wet etching, the indium layer is patterned by a method of lift-off etching.

### 2.5.2 Lift-Off Etching

After the gold is patterned and the mask removed, another layer of photoresist is deposited and patterned such that a window is opened wherever the indium is intended to bond to the underlying gold features.



**Figure 2-25.** Illustration of indium lift-off etch on gold layer of ceramic substrates.

As illustrated in Figure 2-25(c), this is done using the same photolithographic steps described for other techniques. The indium layer is deposited such that it covers all features on the substrate, as shown in Figure 2-25(e), including the top of the photoresist. Since this portion of the substrate is not intended to support indium, this material floats away when the photoresist is etched. As illustrated in Figure 2-25(f), the indium layer remains only where it bonded to the underlying gold features.

## **2.6 Summary**

Although somewhat complex in execution, the concepts of microfabrication presented in this chapter are very basic tools by which miniaturized features are created on a variety of substrates. These procedures are mentioned in the following chapters as a means to create the specific modules used in flip-chip fabrication.



## **CHAPTER 3**

### **OVERVIEW OF FLIP-CHIP ASSEMBLY**

This chapter provides a brief introduction to the flip-chip assembly process and summarizes the short history of the technique. Although only the fundamentals of the baseline process are described in this chapter, all forms of flip-chip assembly reported in this dissertation stem from the same basic concepts.

#### **3.1 Background**

Current surface-micromachining technologies limit MEMS designers to few choices of materials or number of structural layers. More complex structures can be made by flip-chip bonding of surface-micromachined devices onto a variety of material substrates or even other devices. The original silicon host substrate is then removed to produce a highly advanced MEMS that are better suited to radio frequency (RF), microwave, or optical applications where specific material properties are paramount or where more structural layers are required.

Due to the significant leveraging of the Integrated Circuit (IC) industry by MEMS foundries, it is unlikely that any type of non-silicon foundry service will

emerge until it is commercially sound to justify the enormous expense of engineering such a process. However, there are a number of applications that currently exist to which MEMS on non-silicon substrates would be ideally suited. For instance, surface-micromachined variable capacitors would be a significant advancement in tunable filters for RF applications in which a reliable, low-loss, inexpensive, and highly miniaturized devices could be used to precisely tune filters and oscillators.

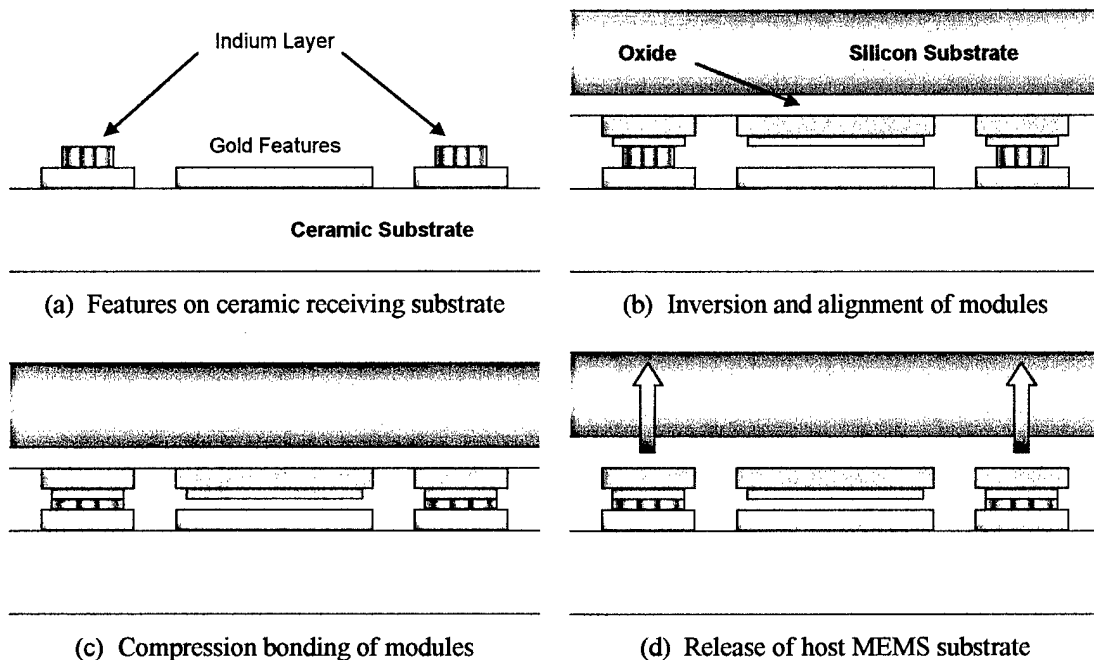
Unfortunately, specifically in the case of RF applications, the silicon substrate upon which the capacitors are typically made significantly interferes with the intended operation of the circuit. This comparably large mass of conductive material demonstrates significant charging effects when implemented in such applications, making the use of such capacitors impossible. Likewise, countless other applications exist without the means of realizing the MEMS that would enable them. For instance, thermal management is a significant issue with respect to excessive heating of sensors and actuators during operation. However, when compared to more ideal material preferences, the standard silicon substrate with a layer of isolation nitride supporting the micromechanical features is somewhat poor for dissipating such heat and will be the critical failure mechanism for a number of high-power applications.

The solution to these problems is to develop a novel post-process assembly technique that would make use of an existing fabrication process. Numerous commercial foundries have already fully optimized the MEMS fabrication processes for increased yield, turn-around time, and reduced cost. Therefore, rather than develop a new fabrication method, a post-process flip-chip assembly technique could be used that would leverage the existing fabrication industry and would be far more

efficient and realizable. Reducing such a flip-chip assembly technique to practice would allow designers to transfer application-specific devices to a variety of desired work surfaces or assemble highly complex devices.

### 3.1.1 Introduction to the Flip-Chip Assembly Process

The flip-chip assembly process is a novel technique by which MEMS structures fabricated by standard surface-micromachining services can be transferred to other substrates or more desirable work surfaces without the original substrate upon which it was fabricated. Figure 3-1 illustrates this process using a simple parallel plate capacitor.



**Figure 3-1.** Simplified illustration of a general flip-chip assembly technique.

The general procedure for constructing flip-chip MEMS on non-silicon substrates involves only two post-process steps beyond traditional fabrication procedures. First, the test structures are prefabricated in a commercial foundry service such that the devices are anchored to the original silicon host substrate only by the sacrificial oxide layers encasing it. Then, as shown in Figure 3-1(a), a ceramic substrate is patterned with gold wires and electrodes upon which indium layers are patterned to receive the test structures. As shown in Figure 3-1(b), the host substrate containing the test structures is aligned over the ceramic receiving substrate at which point the two modules are joined together, as shown in Figure 3-1(c), using a variety of thermosonic and thermocompression bonding techniques. Finally, the bonded structure is then released, as shown in Figure 3-1(d), to free the test structures and remove the silicon host substrate which simply floats away in the solution.

### **3.2 Benefits and Motivation**

As expected, there are several specific needs in the MEMS industry that would drive the development of such a technique. Normally, designers have no choice but to accept the limitations of commercial fabrication services such as the number of available layers, the type of substrate used, or the material used as the structural or sacrificial layers to build the devices. With flip-chip assembly, however, greater flexibility is achieved where designers now have a choice of material substrates and the option to integrate additional structural layers.

### **3.2.1 Material Selection**

As depicted in Figure 3-1, a polysilicon capacitor is formed atop a ceramic substrate using a simple structure fabricated in a standard commercial foundry service. The same device could have been created in the MUMPS process with two notable exceptions. First, the gold layer can only be deposited on the upper side of the top polysilicon layer which makes its use for two inner parallel plates impossible. Secondly, the device would still be supported atop a silicon substrate. For many applications, such limitations would preclude the operation of such a device.

For instance, RF applications require very specific materials to prevent adverse effects typically associated with higher frequencies. Silicon substrates, as an example, exhibit charging effects that make RF applications impossible. Likewise, the gold between parallel plates would be required to increase the quality factor ( $Q$ ) of the device. Without these layers, bare polysilicon plates would not be effective. Only by flip-chip assembly is such a device realizable. Likewise, other advanced applications may demand material specifications such as reflectivity, residual stress, or layer thickness that may only be achievable using the flip-chip assembly technique.

### **3.2.2 Microsystem Integration**

One of the most promising benefits of flip-chip assembly is the capability to integrate MEMS and CMOS to create far more advanced microsystems. Unlike standard techniques like MCMs or traditional flip-chip bonding of entire substrates, the flip-chip assembly technique allows improved performance of the MEMS by

directly coupling devices to electronics. For instance, an array of electrostatically actuated micromirrors must have at least two layers to form the upper and lower electrodes of the device. Additionally, wiring each device within large arrays may require at least one more layer to achieve large wiring densities. On the other hand, if that array could be assembled atop an opposing array of latching cells on a CMOS chip, the combined layers and static memory of the two chips would form an advanced, smart microsystem. Individual devices can be activated and latched into position with the digital control electronics integrated on the same chip with the micromirror devices mounted directly over the CMOS address cells.

Similar to other methods of integration, the total number of control lines is dramatically reduced. Normally, one line would be required for each device within the array. With such a flip-chip array, however, only the CMOS electronics need be addressed and can be reduced to a simple row and column address architecture. Therefore, what may have required hundreds or even thousands of address lines and dual packaging with complicated interconnects now consists only of a single chip with only a few input and output connections. Additionally, the overall functionality of the individual devices is drastically improved since the lower address electrodes are fabricated on the CMOS chip instead of a structural MEMS layer and the CMOS oxide layers inherently prevent shorting of collapsed devices.

### 3.2.3 Additional Structural Layers

Another benefit of flip-chip assembly is the ability to create structures with far more layers than any given foundry service provides. It is known that the complexity and therefore capabilities of MEMS increases rapidly with additional structural layers. For instance, a process that offers only one layer can not be used to create advanced micromirror devices. A single additional structural layer can result in a dramatic jump in complexity and functionality of such a device. A structure comprised of only one releasable layer can accomplish only simple tasks such as sensing acceleration. On the other hand, highly advanced structures that have four releasable layers can be designed to perform a variety of complex tasks. In short, the ability of MEMS to perform specific tasks or to allow optimization of functional devices increases drastically with more layers available to designers.

Given this relationship, it is amazing to note that flip-chip assembly can create advanced devices with potentially *dozens* of layers. Each time the flip-chip assembly technique is used, the number of structural layers and complexity of the assembled device increases. For instance, a receiving chip can be designed in the MUMPS process with three structural layers shaped in the form of the lower portion of some complex device. From the same process, a structure with two more layers can be transferred over the previous layers to create a new device with five structural layers. Each time the process is completed, two additional layers are added to the working substrate like building a house one level at a time. As described in Chapter 2, the complexity and capabilities of such a device increase dramatically with each transfer and are limited only by the control of the flip-chip assembly process.

### 3.2.4 Inherent Planarization

One of the most significant drawbacks of surface-micromachining is the effect of topography that is induced on upper layers by features patterned in underlying layers. For instance, a set of flexures that support the surface of a micromirror would normally be fabricated around the edge of the mirror rather than beneath it to avoid severe bumps in the mirror surface that would dramatically reduce the optical efficiency of the device. The demand for maximum optical efficiency makes the issues of local planarity and reduced surface roughness of a micromirror surface critical. The flip-chip assembly process inherently produces almost ideal mirror surfaces because the array is fabricated upside down over a flat layer of oxide. The mirror surface is actually the underside of the first releasable layer and is naturally smooth and flat since it is unaffected by topography.

The surface roughness characterization of typical flip-chip micromirrors shows that these devices boast almost unprecedented optical flatness. Flip-chip micromirrors demonstrate average peak surface variances of only 15.83 nm with an average of only 1.78 nm of RMS surface roughness throughout all of the arrays. Furthermore, the surface of each individual micromirror is so flat that no radius of curvature could be extracted from the surface characterization data. In comparison, the previously mentioned SUMMiT fabrication service uses a highly complex and costly method of Chemical Mechanical Polishing (CMP) to form planarized surfaces. However, even this most advanced commercial process in the country typically demonstrates as much as 150 nm of print-through topography in mirror surfaces [5].



### **3.3 Disadvantages of Flip-Chip Assembly**

Although flip-chip assembly offers a unique method of creating highly complex devices on a variety of materials, it is not yet available without significant disadvantages. The most common and sometimes overwhelming disadvantages include the need for highly specialized and often costly equipment, concern for alignment between flip-chip modules, and the need for a significant amount of sometimes complex preprocessing necessary to form a strong bond between them. At present, these disadvantages are unavoidable, almost always dramatically reduce assembly yield, and have limited the use of this technique by university, industry, and government laboratories. As long as cost remains an issue, it is unlikely that flip-chip assembly will be widely adopted as a feasible means of fabricating advanced MEMS until these primary disadvantages can be overcome.

#### **3.3.1 Specialized Equipment**

In order to bond two flip-chip modules, a complex bonding machine must be built in which the two modules can be aligned and brought into contact while controlling a variety of bonding conditions. To build such a machine is not easy and can be somewhat expensive. The tolerance in each component must be carefully controlled in order to achieve the desired alignment tolerance of MEMS components. The bonding machines built at the University of Colorado at Boulder have undergone several design and evaluation cycles such that the current system has evolved into a very precise, fast, and easy-to-use flip-chip bonding machine. Some of the research

presented in this dissertation was conducted using the original flip-chip bonding machine in which some features of the process such as alignment error were not well controlled. The performance of the final flip-chip structures can clearly be linked to the quality of flip-chip assembly based on the capabilities of the machine on which they were built. Chapter 4 describes the flip-chip bonding machines in greater detail.

### **3.3.2 Alignment Error**

One of the most noticeable and frustrating disadvantages of flip-chip assembly is alignment between the host substrate and the receiving module. The flip-chip bonding machines are comprised of large-scale mechanical components that are intended to position micromachined devices with sub-micron alignment accuracy. Due to the need for the camera system, the flip-chip modules are aligned while still separated by a significant distance. After one module travels that distance, alignment is usually compromised to the extent that the transferred structures are unusable or the bonding does not hold. Although the alignment error can be significantly reduced by repeated calibration and design techniques, the proper alignment between flip-chip modules will always remain a primary concern.

### **3.3.3 Complex Preprocessing**

Another significant disadvantage of some flip-chip assembly techniques is the need for complex preprocessing to bond the two modules. Most of the recent work has involved the use of ceramic substrates for RF applications in which polysilicon

variable capacitors were bonding using thin layers of indium. Unfortunately, this process involves several steps beyond the commercial prefabrication of the capacitors. The ceramic substrate must be patterned with gold wires and the indium must be deposited and patterned atop the gold.

The preprocessing of ceramic substrates requires multiple photolithography stages that demand considerable time and material resources. First, a positive mask must be drawn and printed for the gold wiring pattern on the ceramic substrate which is purchased with a uniform 2  $\mu\text{m}$  thick film of gold. The film must then be used to create a photomask which is used to pattern a layer of photoresist that must be deposited, cured at high temperature, and exposed to UV radiation under an expensive mask alignment machine. Once exposed, the photoresist must be chemically processed to reveal the unwanted gold that must then be chemically etched to form the wiring pattern. The photoresist must then be stripped off in order to form the ceramic substrate with the desired gold wiring pattern.

Once the gold is patterned, the indium adhesion layer must be patterned on the bond pads that will join the two modules. First, a negative mask is drawn for the indium such that the entire mask is black except for open windows where the indium is desired. Again, this film is used to create another photomask which is used to pattern a new layer of photoresist deposited on the ceramic substrate. Once the photoresist is cured, exposed, and developed, a thin film of indium is deposited over the photoresist which adheres to gold that is exposed beneath it. Finally, a “lift-off” photoresist etch removes all indium that is not bonded to gold features on the substrate. Ultimately, this process demands considerable time and materials.

### **3.4 History of Flip-Chip Assembly**

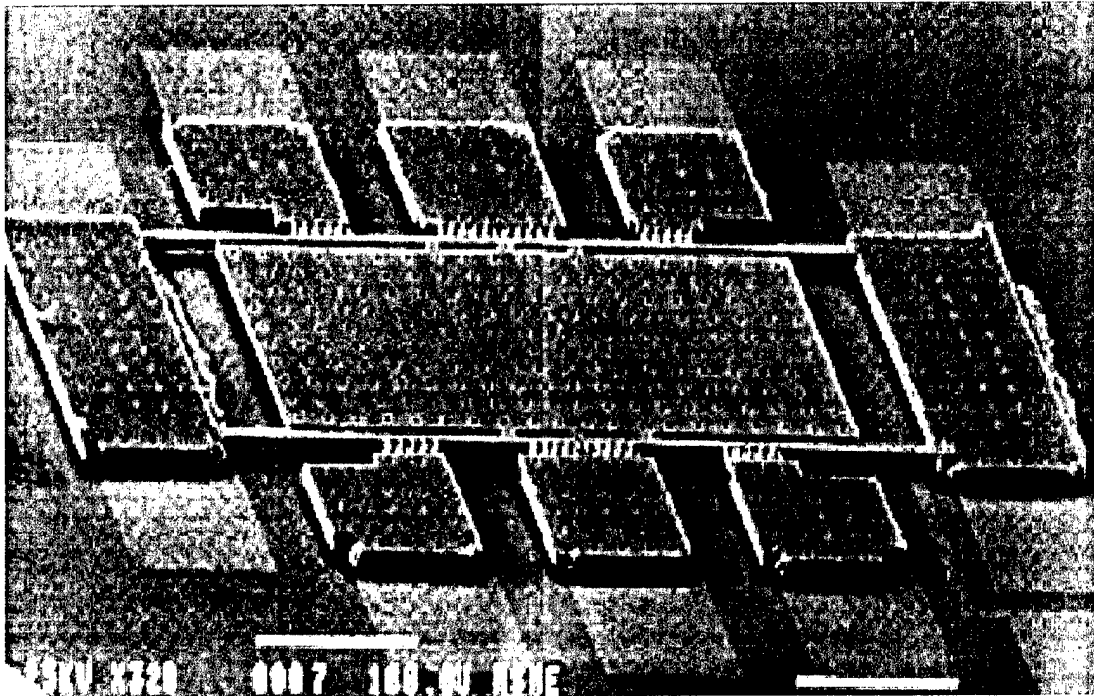
A literature review of flip-chip technology regarding micromechanical devices has revealed that a flip-chip method of fabrication for advanced devices is quite a novel approach. Currently, flip-chip technology is widely used for the integration of electronics and MEMS where a small die of control electronics is flip-chip bonded to a standard MEMS chip [8]. This flip-chip technique is purely a wiring procedure and does not enable advanced micromechanical devices or the use of a variety of material substrates. Alternatively, using this method as a means of fabricating MEMS has only been attempted by two groups of university researchers.

#### **3.4.1 Foundations of Current Research**

Located at the Berkeley Sensor and Actuator Center at the University of California, the first group of researchers has used the flip chip method to transfer MEMS to a new receiving substrate [9]. Figure 3-2 shows a resonating device that was fabricated by such a method. This device was first fabricated in a standard surface-micromachining process and then transferred to a glass substrate using a flip-chip assembly method.

The glass substrate is patterned with bonding pads and wires using any type of conductive material such as gold or copper. Before the transfer, the same material is deposited onto the top of the structure and patterned to form bond pads to match those on the glass substrate. When the device is released and flipped onto the glass substrate, the pads are bonded together using either a direct cold welding or by using

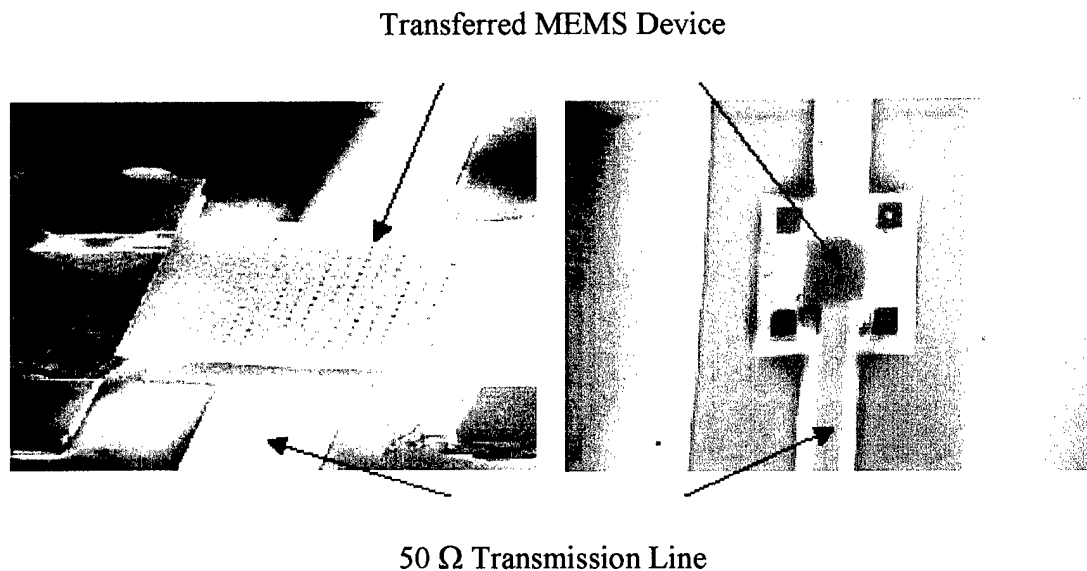
another material, such as indium or lead solder, deposited to act as an adhesive between the pads. Although this process proved capable of producing a few, simple working devices, it was very complex with low yield.



**Figure 3-2.** Micrograph of a resonating structure transferred to a glass substrate [9].

The second group of researchers who have demonstrated this process are located here at the University of Colorado at Boulder. This process has been demonstrated using a simple MEMS device fabricated in the MUMPs process. The first devices fabricated with this technique were simple polysilicon plates connected to bond pads on which gold balls were deposited for bonding. Figure 3-3 shows this simple MEMS device as it is fabricated on the glass substrate.

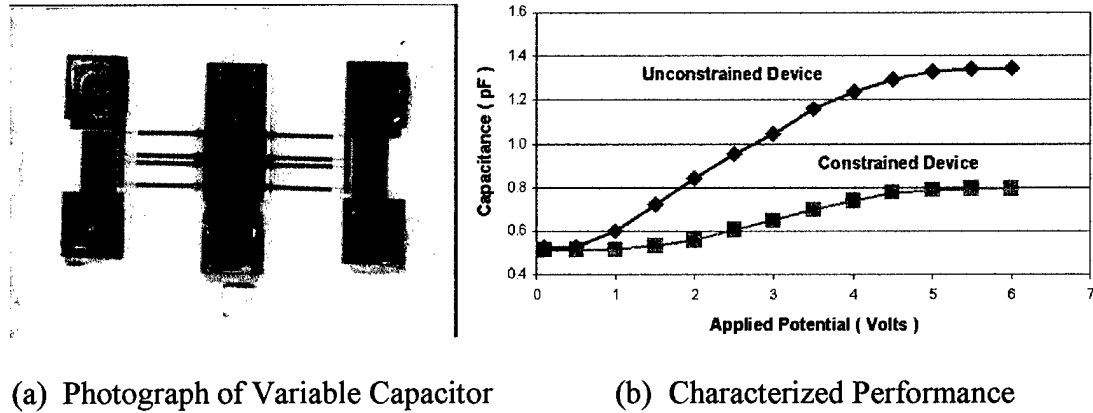
This device is a polysilicon plate suspended over a gold transmission line by four large bond pads. The gold balls were compressed during thermosonic bonding and provide the separation between the two electrodes. This first-generation research has inspired most of the more advanced flip-chip assembly research at the University of Colorado. At the beginning of this research, the device shown in Figure 3-3 was the most complex device fabricated using this method.



**Figure 3-3.** Micrographs of a transferred MEMS device atop a glass substrate [10].

Shortly thereafter, this procedure was expanded to create various devices for RF, optical, microwave, and thermal management applications. For instance, the variable capacitor shown in Figure 3-4(a) was created for RF applications that required specific ranges of capacitance with low address potentials [11]. This particular device uses vertical thermal actuators to raise and lower the upper plate of a parallel plate capacitor that is formed with a gold plate patterned on the ceramic

substrate beneath it. When a potential is applied through the actuators, the upper plate is raised so that the gap between the two plates increases.



(a) Photograph of Variable Capacitor (b) Characterized Performance

**Figure 3-4.** Photograph and performance of thermal actuator variable capacitor [11].

The change in capacitance of two types of devices is characterized versus address potential, as shown in Figure 3-4(b), to reveal a working flip-chip variable capacitor.

### 3.5 Summary

The flip-chip assembly process was developed from a simple concept in which it is easier to transfer a surface-micromachined device onto a desired surface than it is to develop a completely new foundry service. Given the limited prior study of such techniques, there was much to be determined about the process before it can be used to produce complex structures. For instance, flip-chip assembly of some devices such as large micromirror arrays presents special concerns such as planarity and device uniformity throughout the array that may prove difficult to accomplish. It

is easy to see, however, that flip-chip assembly offers significant potential for realizing advanced MEMS and integrated microsystems that simply were not possible in the past. Ultimately, this process has demonstrated the potential to create highly complex devices and allows the use of virtually any host substrate or work surface.



## **CHAPTER 4**

### **EQUIPMENT AND PROCEDURES**

This chapter presents the fundamental equipment and procedures by which the flip-chip modules presented in the following chapters are designed, bonded, and characterized. Since each flip-chip process requires a distinct set of procedures, the steps involved in each portion of the research are outlined within each respective chapter. This chapter presents the fundamental technique by which flip-chip modules are designed and prefabricated and then bonded using one of two flip-chip bonding machines built at the University of Colorado. The procedures by which each form of flip-chip bonding is implemented are either presented with each process or are commonly known techniques that will not be reported.

#### **4.1 General Design of Flip-Chip Modules**

The flip-chip modules presented in the following chapters span several forms of flip-chip bonding that depend on the desired application. For various RF circuit applications, a surface-micromachined host module is prefabricated using a

commercial foundry service and then bonded atop a ceramic substrate to form the final devices that require the ceramic substrate for select material properties.

For submount bonding, a receiving module is also fabricated in the same commercial foundry service in which the two modules are bonded together to form the working device. In this manner, flip-chip structures appear very similar to fully surface-micromachined structures with additional structural layers.

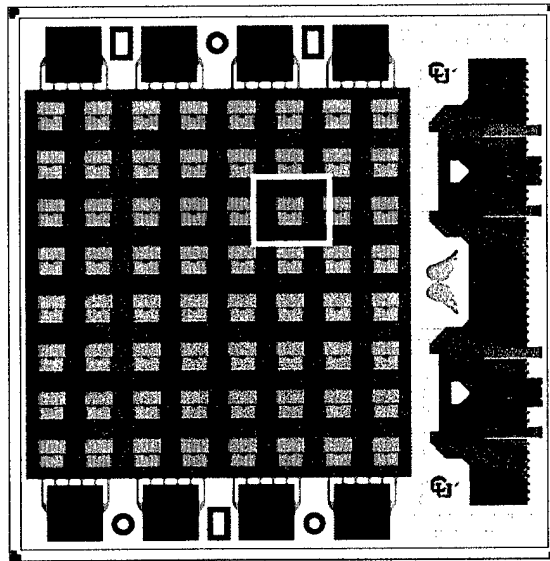
Finally, integrated microsystems can be created by flip-chip bonding the host modules onto CMOS receiving chips. The same commercial foundry service is used to create the MEMS components which are then directly coupled to the electronics.

In all cases of flip-chip bonding presented in this dissertation, a basic concept in the design of these modules is followed such that the final assembly of the desired device is made easier and more reliable. Each of the host modules is designed with the desired layers to be transferred to the receiving module. These upper layers take advantage of the small feature sizes that are common with commercial foundry services such that intricate features can be prepared for flip-chip assembly.

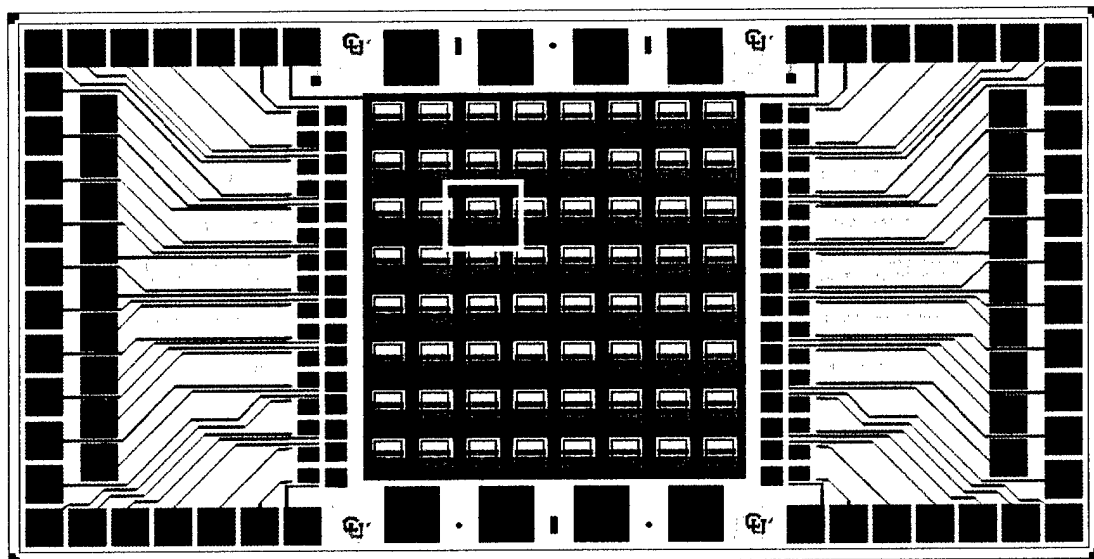
Although the receiving modules differ between each type of assembly, the concept remains the same. The receiving substrate must include receiving bond pads that are placed in a mirror image to those on the host module in order to receive them once the host module is inverted and bonded. Both modules must also contain various alignment marks that not only allow the proper alignment between modules, but also indicate any required orientation between the two sets of features.

These features are illustrated by a typical pair of submount flip-chip modules in which an array of cantilever micromirror devices are to be bonded atop an

opposing receiving array of address electrodes and address wires. Figure 4-1 shows the layout of a typical pair of modules drawn for commercial prefabrication.



(a) Layout of a typical 2 x 2 mm host module



(b) Layout of a typical 2 x 4 mm receiving module

**Figure 4-1.** Layout of typical cantilever submount micromirror flip-chip modules.

In this illustration, a 2 x 2 mm micromirror host module is designed to bond to a larger 2 x 4 mm receiving module. All structures on the modules are drawn within a 50  $\mu\text{m}$  margin to create a 100  $\mu\text{m}$  dicing street between each module. The micromirror cell on the host module typically contains the mirror surface of each final device while the receiver cell on the receiving module typically contains the address electrodes and wiring. The two flip chip modules are drawn as mirror images of each other such that the highlighted micromirror cell in Figure 4-1(a) is bonded atop the corresponding receiver cell highlighted in Figure 4-1(b) once the host module is inverted and bonded.

Both modules typically share a common bonding assembly that usually anchors the mirror surfaces by compliant flexures to a support frame surrounding each device within the array. The features on the host module in Figure 4-1(a) are drawn without rigid anchors to the substrate. Since the arrays are then supported only by the lower oxide layer, the devices separate from the host substrate during the release etch [10]. The spent host module simply floats away once all oxide has been removed. In this example, the resulting devices have five structural layers of polysilicon bonded together with a thin layer of gold.

The off-chip hinge mechanism shown along the right edge of the module in Figure 4-1(a) is used in another form of flip-chip bonding that allows the prerelease of the array before bonding on CMOS receiving modules. That feature is not used in this form of flip-chip assembly and is typically severed with a laser cutter or with a micromanipulator probe prior to thermo-compression bonding.

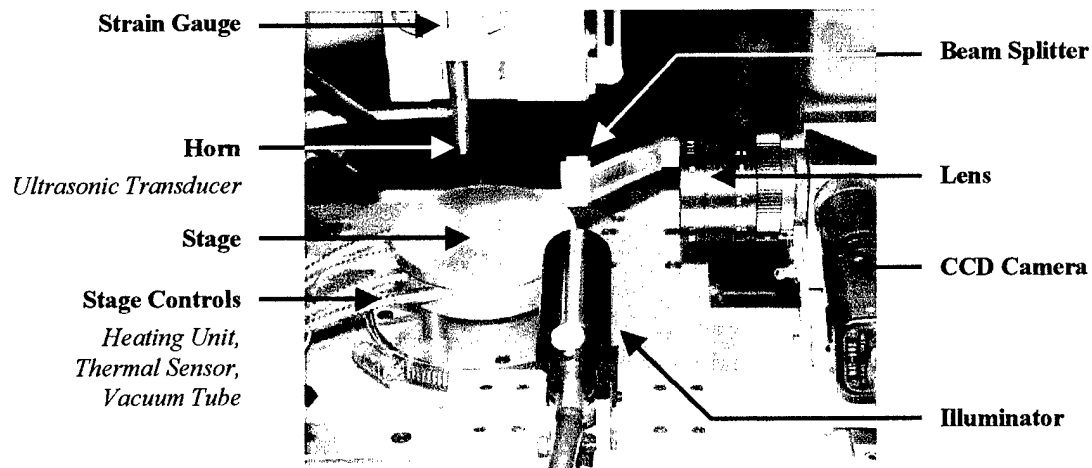
One of the main concerns for any pair of flip-chip modules is the alignment between them once placed on the bonding machine. The two modules shown in Figure 4-1 use a set of asymmetrically distributed pairs of circular and rectangular alignment marks that form the proper pattern in the bonding machine camera system only when the two modules are properly oriented. Since cantilever micromirror devices can only deflect in one direction, the orientation of such arrays is critical. The alignment marks for any flip-chip modules should be adequately spaced to indicate rotation errors.

Once the flip-chip modules have been prefabricated and diced, they are stripped of the protective photoresist in the same manner as standard MUMPs chips. In the case of submount bonding, the only preprocessing step used in the flip-chip fabrication process is a 25 watt argon plasma cleaning for approximately 1 minute which is used to prepare gold bond pads on the modules. Once adequately cleaned, the two modules can be directly fused using the flip-chip bonding machine. Although a variety of bonding materials such as indium and conductive adhesives have been used to assemble devices on ceramic substrates and integrated electronics, the direct bonding of MUMPs modules has proven to be a very simple and effective technique that requires no additional preprocessing of the flip-chip modules.

For other forms of flip-chip bonding, the receiving modules may require some preparation for bonding. For instance, the preprocessing of ceramic substrates discussed in the previous chapters is a long and often difficult process. Although it differs from the submount bonding, the ceramic substrates must also employ alignment marks and similar bond pads to facilitate bonding.

## 4.2 Original Flip-Chip Bonding Machine

The original flip-chip bonding machine used in this research was designed and built many years ago at the University of Colorado. Figure 4-2 shows the working area of this machine which was used to bond host modules atop ceramic substrates.



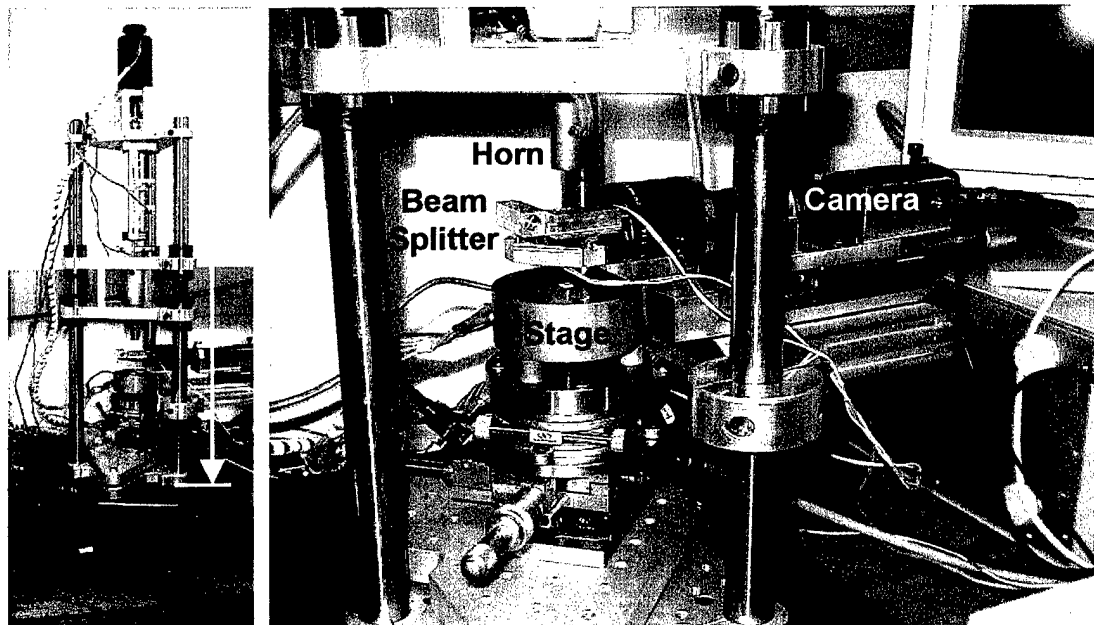
**Figure 4-2.** Photograph of the original flip-chip bonding machine working area.

The working area of the flip-chip bonding machine shown in Figure 4-2 can be broken down into two critical systems. First, the alignment system is comprised of the camera, illuminator, lens, and beam splitter. This system is on a rolling plate that can be used to position the beam splitter directly between the two flip-chip modules such that their superimposed image can be used to align the chips. Finally, the thermosonic bonding system is comprised of the horn, stage, stage controls and strain gauge. Once the two chips are aligned, this system brings them into contact and then monitors the time, temperature, ultrasonic energy and force of the bonding process.

This machine was used only for the original bonding of flip-chip variable capacitors atop ceramic substrates in which a layer of indium was used as an adhesion material. Since the layer of indium was used, the applied stress required to bond the opposing pads was only 25-50 MPa for bonding temperatures ranging from 90°C for small bond pads to roughly 130°C for larger pads. This machine has not been used since the design and fabrication of the new flip-chip bonding machine

### 4.3 Vertical Flip-Chip Bonding Machine

The new flip-chip bonding machine is shown in Figure 4-3 in which the same type of working features are placed in a vertical housing reduced to a table-top unit.



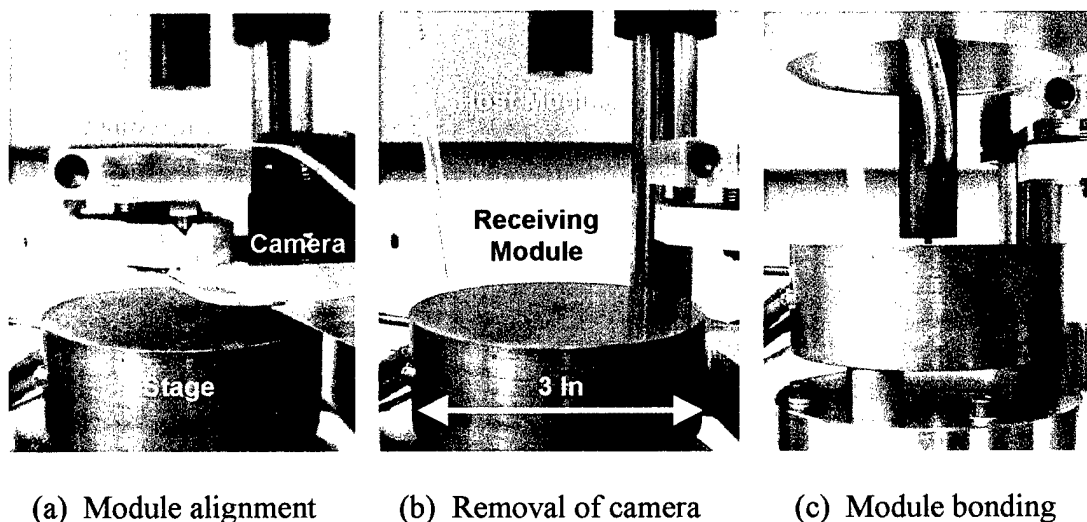
(a) Wide view

(b) Close view of the next-generation working area

**Figure 4-3.** Photographs of the new vertical flip-chip bonding machine.

Based on much of the features found in the original bonding machine, most of the mechanical and optical components were designed and installed with much smaller tolerances in an effort to reduce alignment errors and allow for greater accuracy in computer control. Similar to the original machine, this one consists of a computer-controlled horn that sits directly above a heated translation stage. A camera connected to a beam splitter is inserted between the horn and stage to superimpose the images of the host module and receiving module for alignment prior to bonding.

The stage is heated to the desired temperature between 110°C and 170°C to facilitate the thermo-compression bonding of opposing gold features on the two modules. Higher temperatures are required for larger bond pads and greater number of bonded features while lower temperatures are set for fewer and smaller pads to minimize slip. These bonding parameters are discussed in greater detail in Chapter 7. Figure 4-4 shows several photographs of the flip-chip bonding machine during the standard thermo-compression flip-chip bonding process.

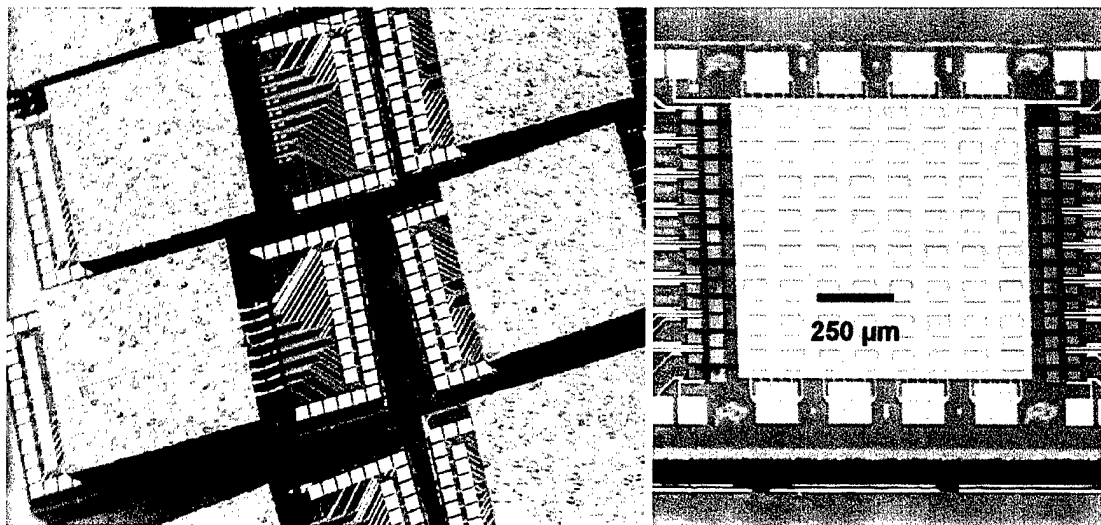


**Figure 4-4.** Photographs of the new bonding machine during the bonding process.



As shown in Figure 4-4(a), the two flip-chip modules are inserted into the bonding machine such that the host module rests inverted under the horn and the receiving module sits directly beneath it on the translation stage. It is preferable to maintain this orientation for all handling of the modules in order to prevent damage during the release etch. Both modules are held in place by a vacuum line.

The rotation and translation controls on the stage are used to align the two modules using their superimposed image viewed through the camera. As shown in Figure 4-4(b), the camera system is then withdrawn to clear the work area of the machine. Finally, as shown in Figure 4-4(c), the computer controls the descent of the horn, the contact force and the hold time for thermo-compression bonding. The modules can be manually bonded if longer hold times are needed. Although not used as part of the baseline flip-chip fabrication process, the computer can also control the level and duration of ultrasonic energy during bonding.



(a) Typical bonded flip-chip modules      (b) Typical released micromirror array

**Figure 4-5.** Photographs of bonded modules and resulting micromirror array.

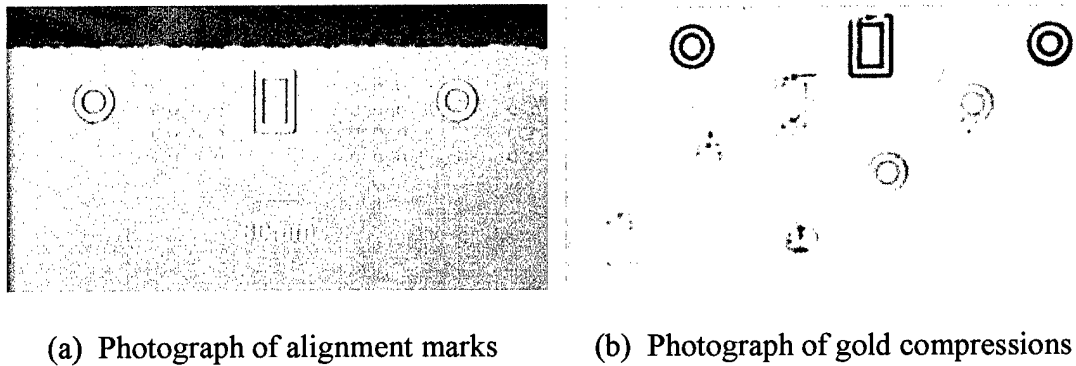
Once the preset bonding force has been reached, the vacuum line holding the host module is disengaged and the horn returns to the original position leaving the bonded modules on the stage. Figure 4-5(a) shows a photograph of several typical bonded modules that are then released to produce highly advanced micromirror arrays like the cantilever array shown in Figure 4-5(b) after the host substrate is removed. This particular array uses eight large bond pads to help support the common bonding frame surrounding each device within the array. Other devices, such as polar piston micromirror arrays, are individually bonded and do not use external bond pads.

One of the potential failure mechanisms of the flip-chip bonding process is the handling of the bonded modules. Most notably, modules that are the same size are susceptible to separation when handled with tweezers. Any contact between them creates sufficient shear stress to break the bonds. As an alternative, Figure 4-5(a) illustrates the use of larger receiving modules so that only the receiving module is manipulated with tweezers or other instruments. As with other modules, this orientation should be maintained throughout all phases of the bonding process.

#### **4.3.1 Periodic Calibrations**

The flip-chip bonding process can be somewhat sensitive to the lateral alignment of the host module features to those on the receiving module or to planarity errors between modules. Slight misalignments can create variations in the device performance while some devices can be rendered completely useless if the alignment error exceeds the tolerance for that device. Likewise, opposing modules may simply fail to bond or even fracture if the planarity error between modules is extreme.

The primary means to regulate the alignment and planarity tolerance and reduce the effects of these errors is simply to conduct repeated calibrations of the bonding machine camera system and translation stage. Both calibrations can be done simultaneously using the same spent host module and ceramic substrate. Figure 4-6 illustrates the first technique by which this calibration is performed.



**Figure 4-6.** Photographs of host module and ceramic substrate calibration test.

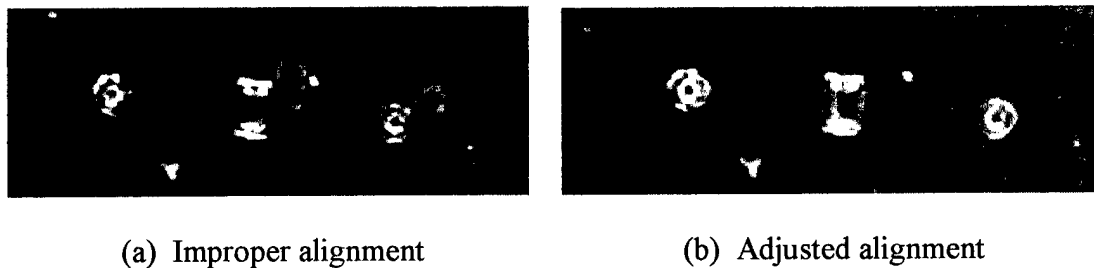
The module shown in Figure 4-6(a) is a typical spent host module in which the micromirror array once supported on the surface has been bonded to a receiving module and released. This module still has the original alignment marks which are fabricated in elevated polysilicon and gold. Now that the array has been removed from the surface of the module, these alignment marks are the only elevated features on the module. Therefore, this module can again be used as a host module and placed on the horn of the bonding machine for calibration purposes.

A ceramic substrate covered in a 2  $\mu\text{m}$  layer of gold is placed on the stage of the bonding machine. This substrate is characterized so that the surface is known to be planar to within a desired tolerance. When the two surfaces bond, the vacuum is

maintained so that the two modules pull apart after bonding without shifting position. When the camera system is again inserted between them, images of the alignment marks and the resulting indentations in the gold layer are superimposed.

At this point, any alignment error in the camera system or planarity error between the modules becomes evident if these features are not fully formed and do not overlap. As shown in Figure 4-6(b), only the far right alignment mark produced a complete indentation in the gold layer on the first bond which indicates a significant planarity error. The bonding is repeated while the tip and tilt controls supporting the stage are adjusted. Successive indentations in the gold layer indicate that the planarity alignment between the modules is improving since all three features are steadily generating the same depth of indentations. Finally, the fourth bond indicates proper planarity. Similar marks on the opposite side of the modules determine whether true module planarity is achieved.

Once the surfaces are planarized, the beam splitter is adjusted until the two sets of features in the superimposed image are aligned. Figure 4-7(a) shows the alignment error and Figure 4-7(b) shows the alignment marks resting within the indentations at which point the calibration of the bonding machine is complete.



**Figure 4-7.** Bonding machine camera system images of opposing alignment marks.

Although this is the main source of error, the position and motion tolerance of other bonding machine components also induce alignment error. Therefore, the flip-chip modules must also be designed to increase alignment tolerance. One of the most effective means to do so is the use of topographically opposed bond pads that bond only when the two pads are adequately aligned. These features are discussed in greater detail in Chapters 7 and 9.

#### **4.4 Summary**

Most of the procedures required to produce flip-chip devices are well known to the designers of MEMS components. For anyone wishing to perform flip-chip bonding, the only new techniques or equipment that must be learned are the general design of flip-chip modules and the fundamental operation of either bonding machine. Although other forms of flip-chip bonding such as CMOS integration or monolithic bonding are also available, these techniques are specifically address in other chapters.

## **CHAPTER 5**

### **CHARACTERISTIC MODELING**

This chapter describes the techniques used to model the behavior of a variety of flip-chip structures such as variable capacitors and micromirror devices. Many of these devices require complex electrostatic models to accurately predict their performance and some are fabricated atop CMOS electronics which add complexity due to multiple dielectric layers. Ultimately, this chapter develops characteristic models of devices ranging from ideal cases to highly complex, integrated systems.

#### **5.1 Introduction**

Developing a model for surface-micromachined capacitors or micromirror devices is as simple as balancing the electrostatic force supplied by the address electrodes with the mechanical restoring force of the flexures supporting the device. In the case of piston devices, the flexures supply a linear spring force [1]. In the case of torsion flexures, an electrostatic torque must be found and equated to the restoring torque of all flexures. In all cases, there is usually considerable variance in material properties and layer thickness of the surface-micromachined structures [12]. As a result, more ideal electrostatic forces and flexure spring forces can be safely assumed.

### 5.1.1 Electrostatic Force

In order to compute the electrostatic force on the upper plate of a device, it must first be determined by which means this force will be calculated. More specifically, it must be decided whether the charge distribution, which is not uniform over the surface, will be considered. The charge distribution will change with the position of the surface and will also be altered by any deformations or discontinuities such as etch holes. This leads to a somewhat complicated solution when integrating across the surface of the device. As an alternative, since both the charge distribution on the surface and the applied electrode voltage are related to the electric field within the device, it is possible to express the potential energy,  $U$ , of the electric charge distribution solely in terms of this field such that

$$U = \frac{1}{2} \int \sigma V dA = \frac{1}{2} \int \epsilon_0 E^2 dv = \frac{1}{2} CV^2 \quad (1)$$

where  $\sigma$  is the surface charge distribution,  $V$  is the voltage between the two opposing plates,  $A$  is the surface area of the mirror,  $\epsilon_0$  is the free space dielectric constant,  $E$  is the electric field intensity at any point in the volume  $v$  within the device, and  $C$  is the total device capacitance [13]. By assigning a relative electric energy density of  $\frac{1}{2}\epsilon_0 E^2$  to each point in space within the device, the physical effect of the charge distribution on the surface is preserved. From this approach it is easy to see that the non-uniform charge distribution on the surface of the device and the fringing electric fields around its edges are complementary descriptions of the same electrical phenomenon.

According to Equation (1), the total potential energy within the device can be found by the surface charge distribution, the electric field within the device, or its total capacitance. As described in the following sections, each approach has unique advantages in specific cases. Regardless of the chosen technique, the force acting on the surface of the device,  $F$ , is found by the gradient of the potential energy such that

$$F = -\nabla U \quad (2)$$

This relationship holds for non-uniform charge distributions and electric fields since the potential energy is found by integrating these respective quantities across the surface and through the volume of the device. As a result of fringing fields around the perimeter, the electric field intensity will be reduced along the edges as will the total force acting on the surface of the device. Using the electric field intensity, the magnitude of the total downward force acting on the surface of the device becomes

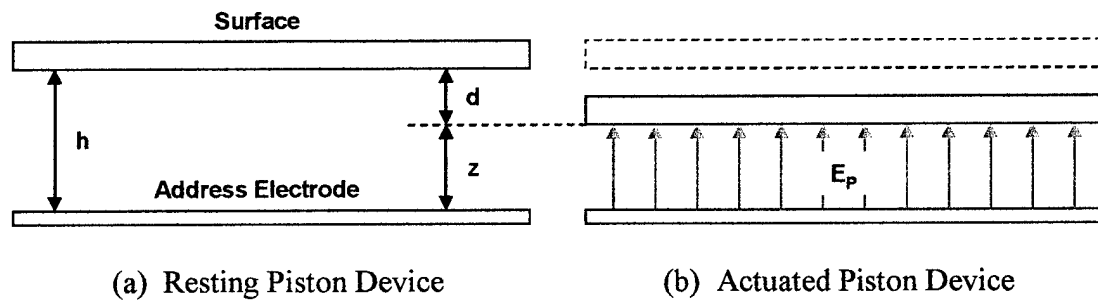
$$F = -\nabla U = -\frac{\partial}{\partial z} \left[ \frac{1}{2} \int \epsilon_o E^2 dv \right] = -\frac{1}{2} \epsilon_o \int E^2 dA = -\frac{1}{2} \epsilon_o \iint E^2(x, y) dx dy \quad (3)$$

which indicates that the distributed electric field is a function of lateral position within the device. This representation will be used to develop the force acting on the surface of both piston and torsion devices. For piston devices, the electric field can often be considered uniform within the device so that the electric field is not a function of position. For torsion devices, the electric field will vary only along one dimension outward from the center of the axis of rotation.



### 5.1.2 Uniform Electric Fields

In the case of piston micromirrors, the mirror surface and a single address electrode form a parallel plate capacitor in which the separation distance between the plates is allowed to change. In short, the capacitance of the device changes with actuation and therefore the electrostatic force varies with the position of the mirror surface. Provided the plates are significantly wider in both dimensions than the gap between them, the electric field within the device can be considered uniform [14]. Figure 5-1 shows a side view of a piston device actuated by a uniform electric field:



**Figure 5-1.** Side view of a resting and electrostatically actuated piston device.

Since the electric field within the device is essentially uniform, it is considered to be orthogonal to the surface of the device at all points beneath it. As a result, the electrostatic force along the surface will act to deflect it directly downward. This assumption neglects deformations in the surface during operation as well as fringing effects of the electric field around the edges of the device. However, the error induced by this idealized approach is much less than the error induced by variances in material properties that are used to predict the behavior of such devices.

From the side view of the device, it is easy to see how the gap between the plates changes with the actuation of the surface. The height of the surface above the address electrode,  $z$ , can be found simply by using

$$z = h - d \quad (4)$$

where  $h$  is the resting mirror height above the electrode when no address potential is applied and  $d$  is the downward deflection of the surface. Based on the assumption of a uniform electric field, the electric field within a piston device,  $E_p$ , is given by

$$E_p = \frac{V}{z} \quad (5)$$

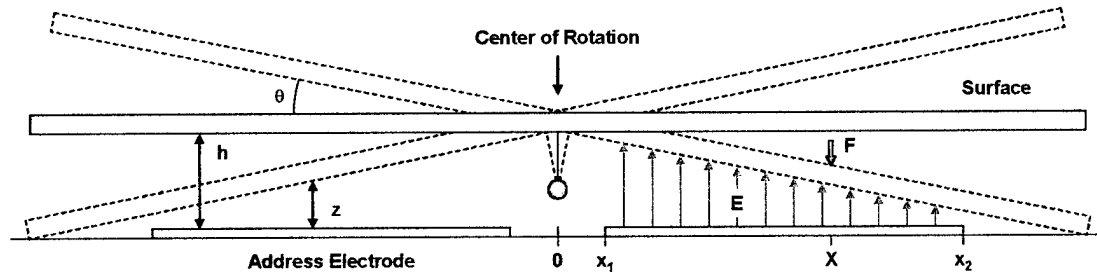
where  $V$  is the address potential applied between the upper and lower plates of the device. Using Equations (4) and (5) to define the electric field in terms of deflection, the total force on the surface of a piston device,  $F_p$ , from Equation (3) yields

$$F_p = -\frac{1}{2}\epsilon_o \int E_p^2 dA = -\frac{1}{2}\epsilon_o E_p^2 A = -\frac{1}{2}\epsilon_o A \left( \frac{V}{h-d} \right)^2 \quad (6)$$

where it is evident that the force will increase significantly as the device deflects downward which eventually leads to electrostatic capture and collapse of the device. This force will be balanced with the restoring spring force of the flexures within the device to produce the working model for piston devices [4].

### 5.1.3 Distributed Electric Fields

Similar to the piston devices, the surfaces of torsion and cantilever devices are electrostatically actuated by an electric field within the device. Unfortunately, these surfaces rotate about a longitudinal axis which creates a non-uniform distribution of the electrostatic force since the separation between the plates is no longer constant. Figure 5-2 shows a side view of such a device in resting and activated states.



**Figure 5-2.** Side view of a torsion device showing the deflection of the surface.

Although there is a very slight forward rotation about which the mirror height changes at  $x = 0$ , the lateral motion of torsion micromirrors is more than sufficiently small to neglect the error. As a result, the height of any point on the mirror surface above the address electrode,  $z$ , can be determined by:

$$z = h + x \tan \theta \quad (7)$$

where  $h$  is the resting mirror height above the electrode when no address potential is applied,  $x$  is the lateral position, and  $\theta$  is the angle of rotation of the mirror surface from the horizontal. It should be noted that deflection toward the positive  $x$  direction

represents a negative angle of rotation and vice versa. As a result, the mirror height will always be less than the resting height along either electrode activating the device.

Recognizing that the electric field does not change in the dimension along to the axis of rotation,  $y$ , the force on a torsion device,  $F_T$ , from Equation (3) reduces to

$$F_T = \int f_T(x)dx = -\frac{\epsilon_o}{2} \iint E_T^2(x,y)dx dy = -\frac{\epsilon_o w}{2} \int E_T^2(x)dx \quad (8)$$

where  $w$  is the width of the address electrode in the  $y$  dimension and  $f_T(x)$  is the distributed force along the  $x$  dimension from the axis of rotation. It is this distributed force function that will be used to determine the total force and the centroid position at which it is applied. As shown in Figure 5-2, the distributed force results in a total force,  $F$ , that is effectively applied as a point force at some centroid position,  $X$ , along the surface of the device that results in an equivalent torque about the axis of rotation. From Equation (8), it is easy to define the distributed force function as

$$f_T(x) = -\frac{\epsilon_o w}{2} E_T^2(x) \quad (9)$$

where the electric field,  $E_T$ , is a function of lateral position,  $x$ , within the device. Similar to the force of a piston device, the electrostatic force of a torsion device is determined by the electric field intensity within it. However, unlike the piston device, the electric field of the torsion device is not uniform and indicates that the distributed force will be greater in regions where the upper plates is closer to the lower plate.

Using the electric field defined in Equation (5) and the relationship in Equation (7), the electric field of a torsion device,  $E_T$ , can be defined at any position within the device. Since the electric field is simply defined by the potential difference,  $V$ , between the plates and the height of the bottom of the surface above the top of the address electrode,  $z$ , the electric field simply becomes

$$E_T(x) = \frac{V}{h + x \tan \theta} \quad (10)$$

The complexity of the torsion device model stems from the intensity of this electric field which varies as the height changes during rotation of the mirror surface. Fortunately, the angle of rotation,  $\theta$ , becomes the independent variable of the final model which reduces much of the complexity of the system.

Substituting the electric field in Equation (10) into Equation (8), the force on a torsion device with a single address electrode reduces to

$$F_T = -\frac{\epsilon_o w}{2} V^2 \int_{x_1}^{x_2} \frac{dx}{(h + x \tan \theta)^2} \quad (11)$$

where the limits of integration are the inner and outer edges of the address electrode, as shown in Figure 5-2, which are defined at positions  $x_1$  and  $x_2$ , respectively. Equation (11) holds for a single address electrode of width,  $w$ , where the force varies only in the  $x$  direction. Segmented address electrodes or those that vary in width require additional forces and centroid positions to determine the total torque.

To solve the force in Equation (11), the definition in Equation (7) is used as a substitution variable where the differential relationship is

$$\frac{dz}{dx} = \tan(\theta) \quad (12)$$

so that Equation (11) reduces to a simple integration given by

$$F_T = -\frac{\epsilon_o w}{2 \tan \theta} V^2 \left( \int \frac{dz}{z^2} \right) = \frac{\epsilon_o w}{2 \tan \theta} V^2 \left( \frac{1}{z} \right) \Big|_{z_1}^{z_2} \quad (13)$$

After substitutions are made to return to the original variable of integration,  $x$ , and evaluating the integral from the original limits of integration, the total force acting on the surface of a torsion device,  $F_T$ , becomes

$$F_T = \frac{\epsilon_o w}{2 \tan \theta} V^2 \left( \frac{1}{h + x_2 \tan \theta} - \frac{1}{h + x_1 \tan \theta} \right) \quad (14)$$

Since the outer edge of the electrode is further from the axis of rotation than the inner edge,  $x_2 > x_1$ , the quantity in brackets in Equation (14) will be positive for negative angles of rotation. Similar to the force acting on the surface of piston devices, given in Equation (6), the total electrostatic force on the surface of torsion devices acts in the downward direction. The force on torsion devices in Equation (14) will also be negative for negative angles of rotation toward the positive  $x$  direction and vice versa.

Once the equivalent point force is known, the centroid position at which it is located must also be found in order to calculate the resulting electrostatic torque. The definition of the centroid position,  $X_T$ , is given as

$$X_T = \frac{1}{F_T} \int_{x_1}^{x_2} x f_T(x) dx \quad (15)$$

where the integral average of the torsion distributed force function,  $f_T(x)$ , produces the position at which the force in Equation (14) is effectively applied [15]. It is the total electrostatic force applied at this centroid position that produces the torque about the axis of rotation that activates the torsion device.

Using the definition of this distributed force function from Equation (9) and the electric field defined in Equation (10), the centroid becomes

$$X_T = -\frac{\epsilon_o w}{2F_T} V^2 \int_{x_1}^{x_2} \frac{x dx}{(h + x \tan \theta)^2} \quad (16)$$

Using Equation (7), the substitution relationship for  $x$  becomes

$$x = \frac{z - h}{\tan \theta} \quad (17)$$

from which the differential relationship in Equation (12) holds true. To solve the integral for the centroid position, Equations (7) and (17) are used to substitute for the

integrand in Equation (16) while Equation (12) is used to replace the original variable of integration. Doing so yields

$$X_T = -\frac{\varepsilon_o w}{2F_T \tan^2 \theta} V^2 \int_{z_1}^{z_2} \frac{(z-h)}{z^2} dz = -\frac{\varepsilon_o w}{2F_T \tan^2 \theta} V^2 \left[ \int_{z_1}^{z_2} \frac{dz}{z} - \int_{z_1}^{z_2} \frac{h}{z^2} dz \right] \quad (18)$$

Performing each integration produces

$$X_T = -\frac{\varepsilon_o w}{2F_T \tan^2 \theta} V^2 \left[ \ln(z) + \frac{h}{z} \right] \Big|_{z_1}^{z_2} \quad (19)$$

which can be simplified using Equation (7) to produce the final solution such that

$$X_T = -\frac{\varepsilon_o w}{2F_T \tan^2 \theta} V^2 \left[ \ln \left( \frac{h+x_2 \tan \theta}{h+x_1 \tan \theta} \right) + h \left( \frac{1}{h+x_2 \tan \theta} - \frac{1}{h+x_1 \tan \theta} \right) \right] \quad (20)$$

where the centroid position is located within the boundaries of the address electrode. As indicated in Equation (15), it should be noted that the centroid,  $X_T$ , is normalized by the total downward electrostatic force supplied by the address electrode,  $F_T$ , which can lead to a difficult solution due to the complicated integrals inherent to both definitions. Although an evaluation of the centroid is useful when designing optimized torsion devices, it is only required when defining the torque about the axis of rotation resulting from the force being applied at the centroid.



The definition of the resulting torque allows the value of the electrostatic force to cancel out which simplifies the solution. The initial definition of torque,  $\vec{\tau}$ , about an axis of rotation is given as

$$\vec{\tau} = \vec{r} \times \vec{F} = |\vec{r}| |\vec{F}| \sin \theta \quad (21)$$

where  $\vec{r}$  is the position vector from the axis of rotation to the position at which the force vector,  $\vec{F}$ , is applied and  $\theta$  is the angle between the two vectors [16]. It should be noted that the plates of a torsion device are separated by a potential difference such that the surface of the device becomes an equipotential line. As such, the electric field lines within the device are always normal to this line which coincides with the underside of the surface. Therefore, the cross product shown in Equation (21) will always be maximized regardless of the angle through which the device is rotated.

The magnitude of the position vector is simply the position of the centroid given in Equation (20) and the magnitude of the electrostatic force is given in Equation (14) so that the torque on a torsion device,  $\tau_T$ , becomes

$$\tau_T = X_T F_T = -\frac{\epsilon_o w}{2 \tan^2 \theta} V^2 \left[ \ln \left( \frac{h + x_2 \tan \theta}{h + x_1 \tan \theta} \right) + h \left( \frac{1}{h + x_2 \tan \theta} - \frac{1}{h + x_1 \tan \theta} \right) \right] \quad (22)$$

It is this electrostatic torque produced by the distributed electrostatic force that will be balanced with the restoring spring torque of the device flexures to produce the final model of a torsion device.

#### **5.1.4 Capacitance**

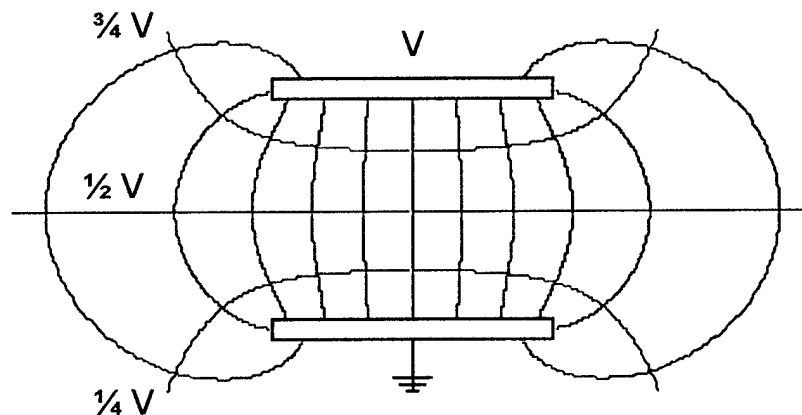
As indicated in Equation (1), the total potential energy stored within a device can also be evaluated using the capacitance of the device. Although the electric field is a simple technique to determine the force on the surface of a device with a single dielectric material between the plates, this approach is more difficult when more than one dielectric material is used. For instance, integrated micromirror arrays are actuated by an electrode encased in oxide on the surface of a CMOS control chip. As a result, the electric field induced within the device spans regions of glass and air which act as two capacitors connected in series. It is possible to find the total capacitance of the device by evaluating the series result of both regions independently. By this approach, Equation (2) can still be used to find the total force acting on the surface of the device by the address potential applied between the two plates. This technique is illustrated in the modeling of integrated piston devices.

### **5.2 Adverse Electrostatic Effects**

The following sections describe some of the most common adverse behavior observed in many electrostatically actuated devices. Although none of the adverse characteristics of test devices listed below is directly incorporated into any of the models developed in this chapter, some become notably significant in certain design variations. Unless specifically prohibited by critical specifications, most of these characteristics can be significantly reduced or even eliminated by design.

### 5.2.1 Fringing Losses

The electric field within a device can be considered uniform if the width of the plates in both dimensions is much greater than the gap separating them [14]. For some variable capacitor designs, however, narrow plates are designed to collapse in a cascading manner to change the total capacitance of the device. These narrow plates are roughly as wide as the gap separating them and will therefore experience significant fringing in the electric field surrounding the edges [14]. As shown in Figure 5-3, the length of the electric field lines increases around the edge of the device while the field lines in the center of the device remain mostly uniform.



**Figure 5-3.** Illustration of fringing electric field lines around the edges of a device.

Since the length of the field lines increases at the edges, the diminished force per unit area will reduce the total electrostatic force. In some extreme cases, narrow devices demonstrating significant fringing experience as much as a 10% reduction from the ideal electrostatic force actuating the surface [14].

### **5.2.2 Cross-Talk**

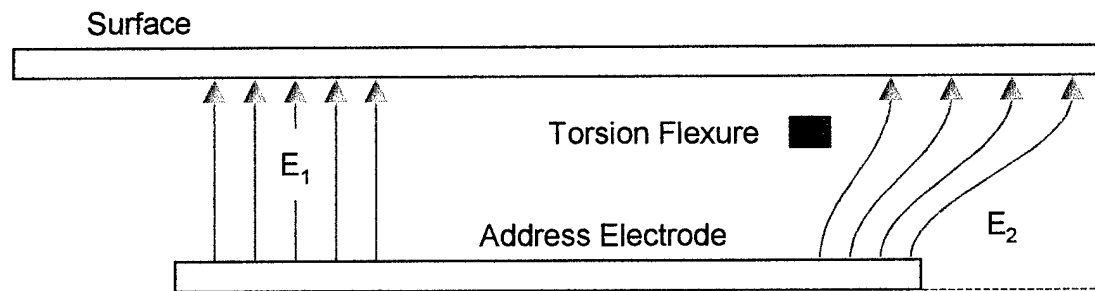
Similar to the fringing electric field lines around the edges of devices, the electric fields of one actuated device may interfere with a neighboring device [14]. For instance, the address potential applied to the electrode of one device within an array may cause the adjacent device to tilt or slightly actuate. These effects become more significant as devices are placed in close proximity within the array and as the gap between plates increases [14]. One of the simplest techniques to eliminate such adverse behavior is to build grounded columns between devices so that the electric field lines from one device are terminated before interfering with another device. Such technique was used in many flip-chip devices discussed in later chapters.

### **5.2.3 Surface Charging Effects**

One of the most common problems associated with the operation of torsion or cantilever devices is the effect of charge accumulation around any areas in which the surface of the device makes contact with the substrate on which it is fabricated [14]. Most notorious for such effects is the silicon nitride layer that is typically used for isolation between the silicon substrates and polysilicon features of most fabrication services. This surface demonstrates such significant charging effects that many devices literally stick in the deflection position until the charge is removed. The springs forces of the device simply are not sufficient to free the surface. As a result, most advanced devices will employ a grounded landing pad to support the surface in the deflected position such that no charging effects will interfere with its operation.

### 5.2.4 Opposing Electrostatic Forces

Although most torsion devices are almost ideally designed with only one address electrode that extends well beyond the torsion axis of the device, there are numerous other designs in which electrostatic forces that oppose the desired motion of the device must be considered. For instance, a cantilever device having a torsion flexure is designed to tilt in only one direction. If any portion of the address electrode is placed beneath the flexure, the intended electric field induced on the surface of the device will also extend to the opposite side of the device. Figure 5-4 illustrates this concept showing a cantilever device with oversized address electrode.



**Figure 5-4.** Side view of typical cantilever device with oversized address electrode.

This device has an electrode that extends slightly into the region on the opposite side of the device. The intended electric field,  $E_1$ , will produce the desired electrostatic force and therefore a torque about the torsion flexure. On the opposite side of the torsion flexure, however, the stray electric field lines extending from the address electrode,  $E_2$ , will induce an opposing torque that reduces the desired effect of the address electrode. Although this effect is usually insignificant, some models must account for these forces unless a ground plane is used to shield the opposing surface.

### 5.3 Piston Actuation

The root of the model for a piston device rests in balancing the restoring spring force of the flexures supporting the surface with the electrostatic force induced by an address potential applied to the address electrode beneath it. The majority of the piston model has been previously developed and will not be reported in great detail in this dissertation [14].

In short, the restoring spring force,  $F_s$ , produced by springs displaced a distance,  $d$ , from the equilibrium position is given by Hooke's Law such that

$$F_s = kd \quad (23)$$

where  $k$  is the characteristic spring constant of the entire system [4]. This constant is the total of the spring constants of all flexures supporting the surface of the device. In order for the surface to deflect uniformly, all flexures must be identical and evenly distributed around the surface.

If the equilibrium position of the surface is defined as the deflection that counters the downward force of gravity on the surface, Newton's second law can be applied to the remaining balanced forces on the system such that

$$F_s + F_p = kd - \frac{1}{2} \epsilon_o A \left( \frac{V_p}{h-d} \right)^2 = 0 \quad (24)$$

where the downward electrostatic force on the surface of the piston device,  $F_p$ , is given in Equation (6) such that there is no deflection ( $d = 0$ ) at equilibrium [16]. For

the system to be balanced by the two forces, there must be no net force and therefore no acceleration of the surface of the device. After substituting the appropriate forces in to Equation (24), the characteristic model of the piston device becomes

$$\frac{1}{2}\epsilon_o A \left( \frac{V_P}{h-d} \right)^2 = kd \quad (25)$$

which can be solved for the address potential,  $V_P$ , required to deflect the surface of the device a distance,  $d$ , from the resting position such that

$$V_P = (h-d) \sqrt{\frac{2kd}{\epsilon_o A}} \quad (26)$$

This idealized model of piston deflection does not include the effects of temperature, surface deformations, cross-talk, fringing electric fields, squeeze-film damping or the frequency response of the device as a simple harmonic oscillator. These complex and often negligible characteristics have been previously addressed for similar devices and will not be developed in this dissertation [14].

As described above, the characteristic device spring constant,  $k$ , can be experimentally determined for a specific piston device. However, mechanical analysis of the geometry and material properties comprising the flexures can approximate this value. As a result, the behavior of a piston device can be predicted without the need for experimental observations.

The beams of the flexures supporting the surface are analyzed as beams that are rigidly supported on one end and free on the other. The primary term of the device spring constant is a cross-section spring constant,  $k_{cs}$ , that relates a downward force,  $F$ , applied at the end of the beam where the maximum deflection,  $d$ , from the horizontal is known. This relationship is given as

$$d = \frac{FL^3}{3EI} \quad \text{and} \quad I = \frac{1}{3}wt^3 \quad (27)$$

where  $I$  is the bending moment of inertia of a beam with rectangular cross-section. The flexure characteristics are represented as  $L$ ,  $w$ ,  $t$ , and  $E$  which are the length, width, thickness, and modulus of elasticity for the beam, respectively [17]. Using Equation (23) to solve for the spring constant yields

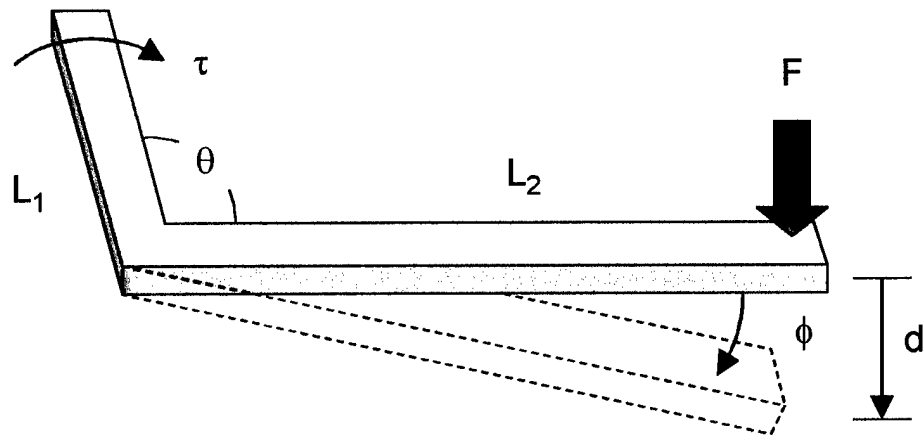
$$k_{cs} = \frac{Ewt^3}{L^3} \quad (28)$$

It should be noted that a considerable variance in the material properties and actual dimensions of drawn features exists between commercial foundry services. As a result, the spring constant can be a source of moderate error unless the properties of a specific foundry service are well known.

In addition to standard beam theory, the spring constant of the flexures must account for their layout such that a corner will produce a flexure that is more resistant to deflection than one of the same length that is straight. Even flexures with rounded



corners produce a torque on some sections of the flexure. The restoring torque of that portion of the flexure will reduce the total deflection at the end supporting the surface of the device. Therefore, a torsion spring constant must be added. This spring constant must be evaluated for each corner of the flexure where  $L_1$  and  $L_2$  are the lengths of the primary and secondary portions of the flexure under test, respectively. Figure 5-5 illustrates these portions and the resulting torque induced on the flexure.



**Figure 5-5.** Illustration of the torque induced on a portion of a piston flexure.

The torque,  $\tau$ , induced on the primary portion of the flexure by a force,  $F$ , at the end of the second portion is defined using Equation (21) such that

$$\tau = L_2 F \sin \theta \quad (29)$$

where  $\theta$  is the planar angle between the two portions of the flexure. For most designs, the two segments are orthogonal such that the induced torque is maximized.

Once the flexure reaches equilibrium, the restoring torque of the primary portion of the flexure will support the force at the end of the second portion. This restoring torque on a torsion member is given as

$$\tau = \phi \frac{KG}{L_1} \quad (30)$$

where  $\phi$  is the torsion angle through which the primary flexure is rotated and  $G$  is the shear modulus of the flexure material. The torsion stiffness constant,  $K$ , for torsion members with rectangular cross section is given by

$$K = ab^3 \left[ \frac{1}{3} - 0.21 \frac{b}{a} \left( 1 - \frac{1}{12} \left( \frac{b}{a} \right)^4 \right) \right] \quad (31)$$

where  $a$  is the greater of the width or height of the flexure cross section and  $b$  is the remaining dimension [18].

As illustrated in Figure 5-5, the end of the flexure deflects a distance,  $d$ , as the secondary portion rotates through a small torsion angle,  $\phi$ , such that

$$\sin \phi = \frac{d}{L_2} \cong \phi \quad (32)$$

where the approximation holds for small angles where the deflection at the end of the flexure is much smaller than the length of the second portions of the flexure.

In equilibrium, there is no net torque on the flexure such that the induced torque in Equation (29) is equal to the restoring torque in Equation (30) such that

$$L_2 F \sin \theta = \phi \frac{KG}{L_1} \quad (33)$$

where the torsion angle,  $\phi$ , can be substituted from Equation (32) to produce a relationship between the applied force,  $F$ , and the resulting flexure displacement,  $d$ . According to Hooke's Law in Equation (23), the torsion spring constant,  $k_t$ , becomes

$$k_t = \frac{KG}{L_1 L_2^2 \sin \theta} \quad (34)$$

This torsion spring constant for angled flexures is used to quantify the added stiffness in the spring flexures of a piston device due to the unwanted torsion of the flexure.

Finally, a stress term is added which describes the added stiffness of the flexure due to internal residual stress in the material. This constant,  $k_s$ , is given by

$$k_s = \frac{\sigma(1-\nu)wt}{2L} \quad (35)$$

where  $w$  is the flexure width,  $t$  is the flexure thickness,  $L$  is the flexure length and  $\sigma$  and  $\nu$  are the stress and Poisson ratio of the flexure material, respectively [1]. This term is usually negligible for devices fabricated in high-quality foundry services.

The total spring constant of the device,  $k$ , is found by summing these constants for  $N$  identical flexures within the device. Since the deflection of most piston device is significantly less than the lateral dimensions of the flexures, the total spring constant of the device is very closely approximated by assuming all flexures to be uniformly deflected for all applied address potentials [19]. The total spring constant of the device is found to be

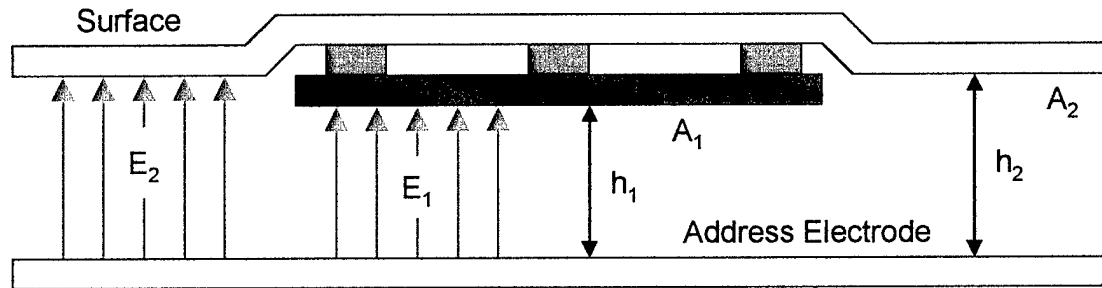
$$k = N[k_{cs} + k_t + k_s] \quad (36)$$

Ultimately, this device spring constant is a function of temperature since the elastic modulus decreases as temperature increases and the thermal expansion of the flexures will slightly alter their geometry [16]. However, such complex behavior has been previously reported and will not be discussed in this dissertation [14].

It is important to note that the cross section constant,  $k_{cs}$ , is typically the dominant term for predicting the device spring constant. However, the stress spring constant,  $k_s$ , becomes more significant when low-quality fabrication services produce devices with tremendous internal stress which dramatically stiffens the flexures. Likewise, some devices use serpentine flexures that wrap through many angles in the layout geometry. The resulting torsion terms from each of the torsion members will increase the torsion spring constant,  $k_t$ , and therefore the total device spring constant. In such a design, the effect of the torsion spring constant can be considerable. A piston flexure with even a single elbow joint will be moderately stiffer than an identical flexure of the same length drawn as a straight beam.

### 5.3.1 Multiple Electric Fields

For some devices with more than one address electrode, the simple piston model given in Equation (26) is not sufficient to model the behavior of the device. For instance, some flip-chip structures have at least two upper plates that form the surface of the device. As a result, the total electrostatic force acting on the surface of the device is produced by more than one electric field within the device. Figure 5-6 illustrates one such device with two levels of upper plates.



**Figure 5-6.** Side view of a flip-chip piston actuator with multiple plate combinations.

Since each region within the device can be separated by a distinct gap between the plates, the electric field in each region and therefore the force per unit area is also unique. For instance, the region with a smaller gap produces a slightly stronger electric field,  $E_1$ , than the other region with a larger gap. It is the combination of these electric fields that produces the total electrostatic force actuating the device. Fortunately, the electric fields are still assumed to be uniform within each region such that the electrostatic force can still be determined by ideal methods.

To find the total electrostatic force on a piston device,  $F_P$ , Equation (6) can be used to determine the force supplied by each electric field independently of the

remaining fields. The application of Newton's second law in Equation (24) would now include the sum of the electrostatic force for each segment. The result yields

$$\frac{\epsilon_o}{2} V_P^2 \sum_{n=1}^N \frac{A_n}{(h_n - d)^2} = kd \quad (37)$$

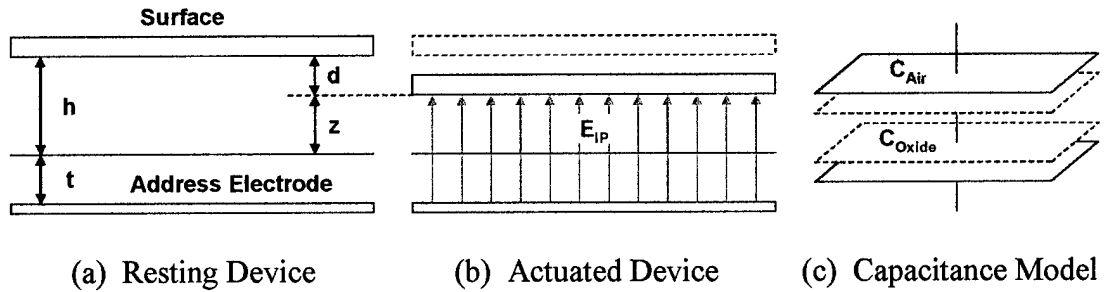
for  $N$  electrode segments having distinct surface area,  $A$ , and resting height,  $h$ , between the two plates of the device. The characteristic model of a piston device with more than one address electrode configuration reduces to

$$V_P = \sqrt{\frac{2kd}{\epsilon_o \sum_{n=1}^N \frac{A_n}{(h_n - d)^2}}} \quad (38)$$

where  $k$  is the total device spring constant given in Equation (36). This model ignores slight variances in the electric fields between regions. Provided the lateral dimensions of each region are much greater than the gap between the two plates and that the difference in the gap between adjacent regions is small, the error induced by the internal fringing fields caused by multiple plates is negligible. Additionally, the area of each section of the surface or address electrode,  $A$ , should represent only the exposed area of that active plate. Only the area that is exposed to the electric field contributes to the force that actuates the device.

### 5.3.2 Multiple Dielectric Layers

Another special case of piston modeling is the integrated device which is bonded atop a CMOS control chip. The address electrode of the device is fabricated on the CMOS chip under a thin layer of oxide. As a result, the gap between the surface and the address electrode is comprised of two dielectric materials. Figure 5-7 shows the operation of such a device including an effective capacitance model.



**Figure 5-7.** Illustration of an integrated piston device with equivalent capacitance.

As shown in Figure 5-7(b), the device deflects normally, but the electric field within the device will be affected by the additional dielectric material and space between the plates. As illustrated in Figure 5-7(c), the capacitance of the integrated piston device,  $C_{IP}$ , is found by evaluating that of the air,  $C_{Air}$ , and oxide,  $C_{Oxide}$ , in series such that

$$\frac{1}{C_{IP}} = \frac{1}{C_{Oxide}} + \frac{1}{C_{Air}} = \frac{t}{\kappa \epsilon_o A} + \frac{z}{\epsilon_o A} \quad (39)$$

where  $A$  is the area of the plates,  $\epsilon_o$  is the free space dielectric constant,  $z$  is the height of the air gap,  $\kappa$  is the dielectric constant of the oxide layer and  $t$  is its thickness.

Although this approach is valid for any second dielectric layer, the dielectric constant for the oxide layer that is typical in CMOS fabrication is roughly the same as glass. With a value of  $\kappa = 6$  for this material, the capacitance of the integrated device will be greater than a device having the same total gap consisting only of air. Solving for the total capacitance of the integrated device yields

$$C_{IP} = \frac{\kappa \epsilon_o A}{t + \kappa z} \quad (40)$$

which reduces to the basic capacitance of a device in air as the thickness of the oxide layer gets smaller. As a result, devices fabricated using CMOS foundry services that have much thinner oxide layers will behave more like standard devices. Using this capacitance in Equation (2), the force on the integrated piston device,  $F_{IP}$ , becomes

$$F_{IP} = -\nabla U = -\frac{\partial}{\partial z} \left[ \frac{1}{2} C_{IP} V^2 \right] = \frac{1}{2} \epsilon_o A \left[ \frac{\kappa V}{t + \kappa z} \right]^2 \quad (41)$$

from which the electric field of the integrated piston device,  $E_{IP}$ , is found to be

$$E_{IP} = \frac{\kappa V}{t + \kappa z} \quad (42)$$

spanning the uniform height  $z$  within the device. This definition of the integrated electric field can also be used to define the varying electric field of a torsion device.



Once the force on the surface of the integrated piston device,  $F_{IP}$ , is known, Newton's second law can be applied as in Equation (24) to develop the final model of the integrated device. Substituting Equation (4) yields the final model such that

$$V_{IP} = \frac{t + \kappa(h-d)}{\kappa} \sqrt{\frac{2kd}{\epsilon_o A}} \quad (43)$$

where  $V_{IP}$  is the address potential required to deflect the surface of the device a desired distance,  $d$ , from the resting position and  $k$  is the total device spring constant.

## 5.4 Torsion Actuation

The root of the model for torsion devices rests in balancing the torque of the twisting flexures with that induced by the electrostatic field along the surface of the device. The restoring torque of a twisted shaft is a simple linear relationship similar to Hooke's Law for linearly displaced springs. The total restoring spring torque,  $\tau_s$ , of  $N$  individual flexures is a function of the torsion rotation angle,  $\theta$ , such that:

$$\tau_s = -Nk\theta \quad (44)$$

where  $k$  is the individual torsion spring constant which is a function of the material properties and geometry of the identical torsion flexures [16]. Typical torsion devices are designed with  $N = 2$  opposing and identical flexures supporting the surface.

The torsion spring constant is used to quantify the stiffness of each flexure and therefore its resistance to twisting. The constant is given by

$$k = \frac{GK}{L} \quad (45)$$

where  $G$  is the shear modulus of the flexure material and  $L$  is the length of the individual flexure [17]. From this equation, it is easy to see that shorter flexures are likely to be more resistant to torsion loads than longer flexures. The torsion stiffness constant,  $K$ , is given in Equation (31) for beams with a rectangular cross section.

To develop the final model of the torsion device, Newton's second law is applied for rotating systems such that no net torque acts on the torsion flexure. In doing so, the magnitude of the electrostatic torque induced on the surface will be equal to that of the restoring torque of the flexure. Unfortunately, the electrostatic torque given in Equation (22) is a function of both the geometry within the device and address potential applied between the plates. In order to separate the address potential as the dependent variable of the final model, the following relation must be defined from Equation (22) such that

$$\psi_T = \frac{\tau_T}{V_T^2} = -\frac{\epsilon_o w}{2 \tan^2 \theta} \left[ \ln \left( \frac{h + x_2 \tan \theta}{h + x_1 \tan \theta} \right) + h \left( \frac{1}{h + x_2 \tan \theta} - \frac{1}{h + x_1 \tan \theta} \right) \right] \quad (46)$$

where  $\psi_T$  represents the voltage normalized torque on a torsion device which reduces to a function of the angle of rotation,  $\theta$ , and the geometry of the address electrode.

Finally, Newton's second law for rotational systems is applied using the electrostatic torque in Equation (46) and the restoring spring torque in Equation (44). Doing so yields the characteristic equation of a torsion device:

$$\tau_T + \tau_S = \psi_T V_T^2 - Nk\theta = 0 \quad (47)$$

which can be solved using Equation (45) for the final model of a torsion device having  $N = 2$  identical torsion flexures such that

$$V_T = \sqrt{\frac{2GK\theta}{L\psi_T}} \quad (48)$$

which describes the address potential,  $V_T$ , required to rotate the surface of a torsion device to a desired angle,  $\theta$ , from the resting position. The voltage-normalized torque,  $\psi_T$ , is given in Equation (46) and is also a function of the rotation angle so that the final model is a complex function of  $\theta$  as the independent variable.

#### 5.4.1 Multiple Address Electrodes

Many versions of torsion devices have stepped address electrodes in order to reduce the address potential of the device. Doing so lowers the separation distance between the plates in the central portion of the device where the mirror surface does not deflect as much as the outer edge. The root of the model for such a torsion device rests in balancing the torque of the twisting flexures with that induced by  $N$  address

electrode segments beneath the rotated surface. Applying Newton's second law for rotating systems shows that the total electrostatic torque induced about the torsion flexure is simply the sum of the torques supplied by each electrode segment.

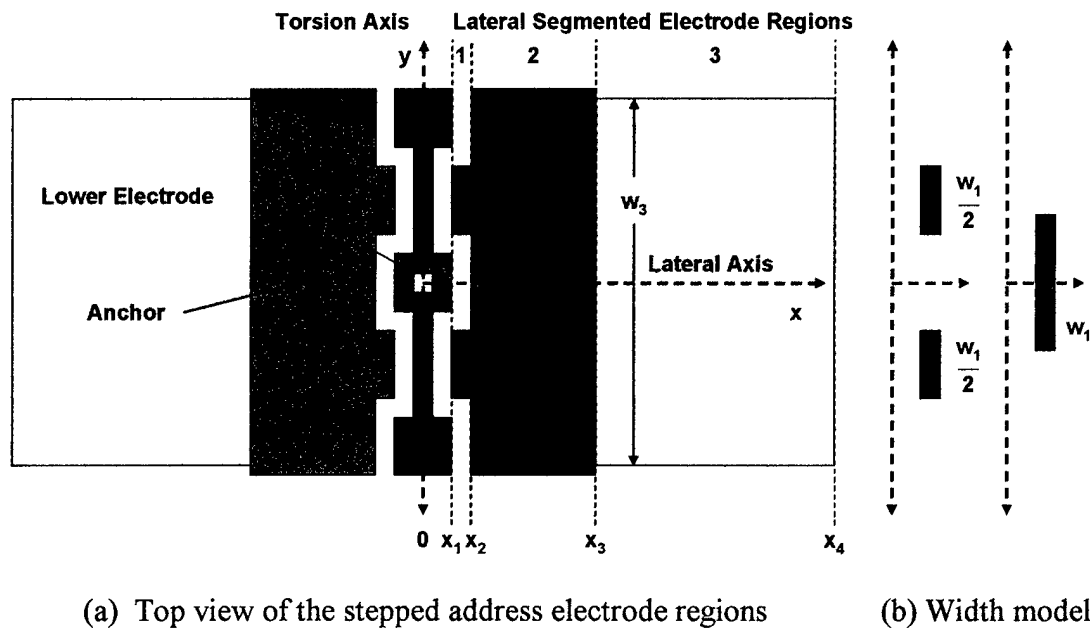
Since each segment of the electrode can vary in height, width and length, each segment will create a distinct distributed force beneath the surface of the device. As a result, each segment will apply a distinct electrostatic force at a distinct centroid position within the boundaries of that segment. The result is a distinct torque induced on the torsion flexures. Once the force and centroid are known for each segment, the total torque induced on the flexures is found simply by

$$\tau_T = \sum_{n=1}^N X_n F_n = \sum_{n=1}^N \tau_n = V_T^2 \sum_{n=1}^N \psi_n \quad (50)$$

where  $n$  is the index spanning  $N$  segments of the address electrode. Again, since each segment of the address electrode is held at the same potential, the voltage-normalized electrostatic torque,  $\psi$ , is defined so that the address potential,  $V_T$ , can be found as the dependent variable of the final model.

The stepped address electrodes within such torsion devices are typically designed to maximize the available surface area in order to reduce the address potential. In such a case, the width of each segment must be carefully defined so that the total area represented by the model is the same as the physical surface area of the address electrode. In order to reduce the model to a function along a single lateral dimension,  $x$ , the address electrode must be segmented into  $N$  distinct regions within which the width of the electrode segment and the resting height of the surface above

the segment are constant. Any variance in either quantity must be evaluated as a separate portion of the electrode. Figure 5-8 illustrates such a device in which the entire address electrode requires segmentation into distinct lateral regions:

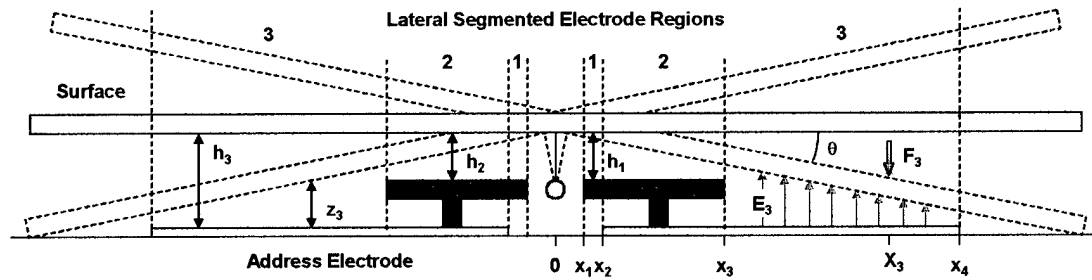


**Figure 5-8.** Illustration of a torsion device with stepped address electrodes.

The address electrodes shown in Figure 5-8(a) are optimized to conform to the flexure assembly that supports the surface through the post at the center of the device. As a result, the segmented region of the address electrode nearest to the torsion axis is divided into two portions that both span the same lateral region. Although each segment can simply be calculated separately, this poses additional complexity when using typical modeling software that deals with lateral position as the integration variable. To reduce complexity, the width of the two sections of the region can simply be added provided they are symmetrically placed about the lateral axis. Doing

so yields a solution for the equivalent torque of the entire lateral region while mathematically spanning it once as though the region consisted of a single electrode segment. Figure 5-8(b) illustrates this reduction with two equivalent electrode segment configurations which produce the same torque about the torsion axis.

The segmented electrode design in Figure 5-8(a) requires a distinct torque to be found for each of three lateral segmented regions. Figure 5-9 shows a side view of the same device and illustrates the reduction of a distributed electrostatic force to the effective point force,  $F_3$ , at the centroid position,  $X_3$ , within the third region:



**Figure 5-9.** Side view of a torsion micromirror with stepped address electrodes.

The electric field within the third lateral region,  $E_3$ , generates a distinct distributed electrostatic force acting on the surface of the device and thereby produces its own torque about the torsion axis shown at the  $x = 0$  position. As represented in Equation (50), the total electrostatic torque about the torsion axis is found simply by adding the torque of each of these individual electrode segments. Although the resting height of the first two segment regions shown in Figure 5-9 are equal,  $h_1 = h_2$ , the width of these regions shown in Figure 5-8 are not equal,  $w_1 < w_2$ , which requires the regions to be analyzed separately.

Similar to a torsion device having only one address electrode, the gap between the surface of the device and the address electrode will vary for each segment by

$$z_n = h_n + x \tan \theta \quad (51)$$

where a rotation toward the positive  $x$  direction is regarded as a negative angle. The resting height of each segment can easily be determined from the layer thickness data provided by the foundry. Figure 5-9 illustrates these dimensions within the device and the relationship between the height of the surface and the rotation angle.

Since each of the electrode segments contributes a distinct torque, each must be evaluated in the same manner as the single electrode of the basic torsion device. In this case, each of  $N$  total voltage-normalized torque values must be evaluated. Using Equation (46), the definition for the  $n^{th}$  electrode segment is given as

$$\psi_n = -\frac{\varepsilon_o w_n}{2 \tan^2 \theta} \left[ \ln \left( \frac{h_n + x_{n+1} \tan \theta}{h_n + x_n \tan \theta} \right) + h_n \left( \frac{1}{h_n + x_{n+1} \tan \theta} - \frac{1}{h_n + x_n \tan \theta} \right) \right] \quad (52)$$

For each segment of the electrode, this quantity is evaluated from  $x_n$  to  $x_{n+1}$  as illustrated in Figure 5-8 and Figure 5-9 which represent the lateral position of the inner and outer edge of each electrode segment, respectively. Typically, the outer edge of one electrode coincides with the inner edge of the next segment. However, devices with larger lateral gaps in the electrodes should be evaluated with the actual limits so that the voltage-normalized torque is valid for each segment.

The characteristic model of a torsion device with stepped address electrodes is created by again equating the restoring torque of the torsion flexures with the net torque induced by the address electrode segments. Using Equations (44) and (50) and solving for the address potential,  $V_T$ , yields

$$V_T = \sqrt{\frac{2GK\theta}{L \sum_{n=1}^N \psi_n}} \quad (53)$$

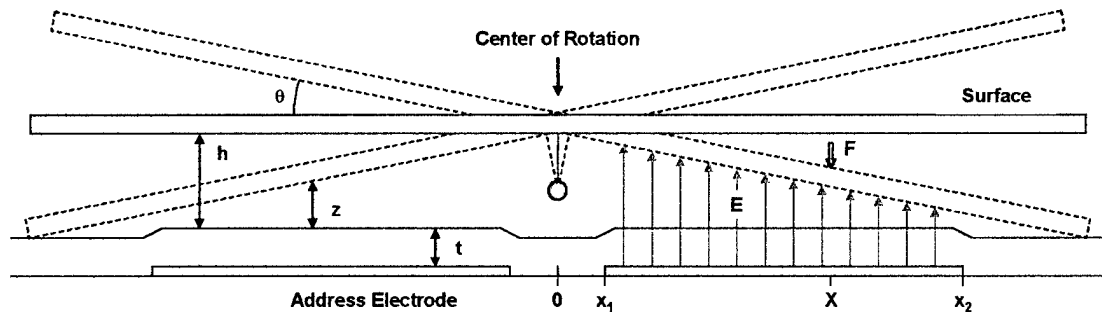
where  $n$  is the index spanning  $N$  segments of the address electrode. The voltage-normalized torque,  $\psi$ , for each segment is given in Equation (52) and is also a function of the rotation angle so that the final model is a complex function of  $\theta$  as the independent variable. It is important to note that a negative rotation angle,  $\theta$ , corresponds to this quantity evaluated for positive  $x$  values so that the entire root in Equation (53) is of a positive number.

#### 5.4.2 Multiple Dielectric Layers

Similar to the integrated piston device, many arrays of integrated torsion devices were fabricated such that the surface of the device rests above an address electrode fabricated on a CMOS control chip. The electrode is covered with a thin layer of oxide such that the gap between the electrode and the surface of the device spans a region containing two dielectric materials. As a result, the intensity of the electric field induced on the surface of the device will be slightly modified.



The gap between the plates is comprised of a thin layer of oxide atop the address electrode on the CMOS chip and the air separating the CMOS chip and the surface of the device. The distributed electric field within the device will exert a greater force per unit area on the surface than a device operating only in air with the same total resting height. Figure 5-10 illustrates the operation of such a device.



**Figure 5-10.** Side view of an integrated torsion device with two dielectric layers.

Again, the root of the model for a torsion device rests in balancing the torque of the twisting flexures with that induced by the distributed electrostatic force of the address electrode beneath the rotated surface [14]. For such integrated devices, the oxide layer over the electrode on the CMOS module produces a total capacitance given by that of the air gap and the oxide layer in series.

Similar to standard devices, the uniform electric field intensity defined for a piston device can be used to define the distributed electric field intensity of a torsion device in which the separation distance between the plates is now a function of position along the surface. Integrating the electric field intensity across the surface produces a different total force for the torsion device versus the piston device.

From the original definition of the distributed force function in Equation (9), the electric field within an integrated device in Equation (42) is modified to define the distributed force of an integrated torsion device,  $f_{IT}$ , such that

$$f_{IT}(x) = \frac{\epsilon_o w}{2} E_{IT}^2(x) = \frac{\epsilon_o w}{2} \left[ \frac{\kappa V}{t + \kappa z} \right]^2 = \frac{\epsilon_o w}{2} \left[ \frac{\kappa V}{t + \kappa(h + x \tan \theta)} \right]^2 \quad (54)$$

using the definition in Equation (7) for the air gap between the plates,  $z$ , as a function of lateral position. From the definition of total electrostatic force from Equation (8), the total force acting on an integrated torsion device,  $F_{IT}$ , is given as

$$F_{IT} = - \int_{x_1}^{x_2} f_{IT}(x) dx = - \frac{\epsilon_o w}{2} \kappa^2 V^2 \int_{x_1}^{x_2} \frac{dx}{(t + \kappa(h + x \tan \theta))^2} \quad (55)$$

Likewise, the centroid position of the integrated torsion device,  $X_{IT}$ , can be found using the original definition in Equation (15) such that

$$X_{IT} = \frac{1}{F_{IT}} \int_{x_1}^{x_2} x f_{IT}(x) dx = \frac{\epsilon_o w}{2 F_{IT}} \kappa^2 V^2 \int_{x_1}^{x_2} \frac{x dx}{(t + \kappa(h + x \tan \theta))^2} \quad (56)$$

Evaluating these quantities is often quite useful when optimizing integrated torsion devices where maximum torque is required. The limiting factor in designing such devices is usually the maximum address potential of the CMOS circuitry driving them, so maximizing either quantity will increase the induced torque on the device.

Rather than evaluating each quantity independently, the product produces a simplified solution. As originally illustrated with the standard torsion device, the total torque is the product of the force and centroid so that the definition reduces to

$$\tau_{IT} = X_{IT} F_{IT} = \int_{x_1}^{x_2} x f_{IT}(x) dx = \frac{\varepsilon_o w}{2} \kappa^2 V_{IT}^2 \int_{x_1}^{x_2} \frac{x dx}{(t + \kappa(h + x \tan \theta))^2} \quad (57)$$

In order to simplify the integral and the solution thereof, the following substitution is defined for the denominator of the integrand

$$u = t + \kappa(h + x \tan \theta) \quad (58)$$

which produces the new definition of the variable of integration:

$$x = \frac{u - t - \kappa h}{\kappa \tan \theta} \quad (59)$$

and the resulting differential relationship:

$$dx = \frac{du}{\kappa \tan \theta} \quad (60)$$

which are both substituted into Equation (57) along with Equation (58) in order to simplify the solution to the integral for the total torque.

The range of integration of the simplified solution is determined from the substitution give in Equation (58) such that

$$\tau_{IT} = \frac{\varepsilon_o w}{2} \kappa^2 V_{IT}^2 \int_{u_1}^{u_2} \left( \frac{u-t-\kappa h}{\kappa \tan \theta} \right) \left( \frac{1}{u^2} \right) \frac{du}{\kappa \tan \theta} \quad (61)$$

which reduces to the difference of two simple integrals such that

$$\tau_{IT} = \frac{\varepsilon_o w}{2} \left( \frac{V_{IT}}{\tan \theta} \right)^2 \left[ \int_{u_1}^{u_2} \frac{du}{u} - (t + \kappa h) \int_{u_1}^{u_2} \frac{du}{u^2} \right] \quad (62)$$

Performing each integration and substituting the limits of integration yields the final solution for the torque induced on the surface of an integrated torsion device such that

$$\tau_{IT} = \frac{\varepsilon_o w}{2} \left( \frac{V_{IT}}{\tan \theta} \right)^2 \left[ \ln \left( \frac{u_2}{u_1} \right) + (t + \kappa h) \left( \frac{1}{u_2} - \frac{1}{u_1} \right) \right] \quad (63)$$

where the values of  $u_1$  and  $u_2$  are defined by Equation (58) such that

$$u_1 = t + \kappa(h + x_1 \tan \theta) \quad u_2 = t + \kappa(h + x_2 \tan \theta) \quad (64)$$

which represent the effective separation distance between the surface of the device and the address electrode if only a single medium of air existed between the plates.

To complete the model of the integrated torsion device, Newton's second law for rotating systems is once again applied such that the sum of the total electrostatic torque in Equation (63) and the restoring spring torque in Equation (44) is zero. Doing so yields the characteristic behavior of the integrated torsion device such that

$$-\frac{\epsilon_o w}{2} \left( \frac{V_{IT}}{\tan \theta} \right)^2 \left[ \ln \left( \frac{u_2}{u_1} \right) + (t + \kappa h) \left( \frac{1}{u_2} - \frac{1}{u_1} \right) \right] = \frac{NGK}{L} \theta \quad (65)$$

where the angle of rotation,  $\theta$ , is still regarded as negative for rotation toward the positive  $x$  direction and vice versa. The final model of the device is found by solving for the address potential of the integrated torsion device,  $V_{IT}$ , such that

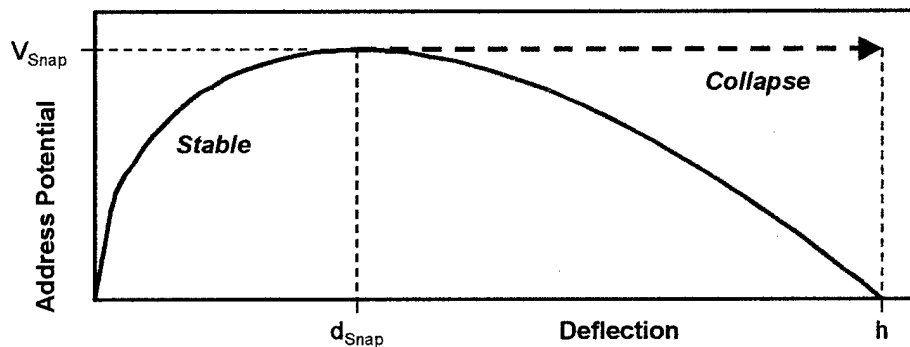
$$V_{IT} = \sqrt{\frac{-2NGK\theta \tan^2 \theta}{\epsilon_o w L \left[ \ln \left( \frac{u_2}{u_1} \right) + (t + \kappa h) \left( \frac{1}{u_2} - \frac{1}{u_1} \right) \right]}} \quad (65)$$

where the quantities  $u_1$  and  $u_2$  are defined in Equation (64) as functions of the same angle of rotation. As a result, the address potential,  $V_{IT}$ , required to rotate the surface of an integrated torsion device to a desired angle of rotation,  $\theta$ , is a very complex function of that independent variable. Again,  $K$  is the torsion stiffness constant given in Equation (41) for each of  $N$  identical flexures. As illustrated in Figure 5-8 showing a standard torsion device, typical devices consist of a surface supported at the center by  $N = 2$  identical and opposing torsion flexures

## 5.5 Electrostatic Capture

One of the primary characteristics of electrostatically actuated devices is the effect of electrostatic capture of the surface. As illustrated in Equation (6), the electrostatic force on the surface increases exponentially as the gap between the two plates decreases during actuation. The restoring spring force of the flexures, however, is simply a linear relationship with deflection. As a result, the device will deflect to some point where the electrostatic force overtakes the spring force and the device will collapse. Beyond that point, the springs are simply not capable of supplying sufficient force to counter the electrostatic force from the address electrode.

If the piston device model in Equation (26) is plotted for a full range of deflection from zero to the full resting height of the device, as shown in Figure 5-11, it is noted that the address potential is maximized at some critical deflection.



**Figure 5-11.** Plot of typical piston device address potential versus surface deflection.

This critical point of deflection,  $d_{Snap}$ , is where the electrostatic force captures the surface of the device which immediately collapses such that the deflection is equal to the original resting height,  $h$ , of the surface above the address electrode.

Since electrostatically actuated devices are stable at deflections less than the collapse deflection,  $d_{Snap}$ , it is useful to predetermine this position to maintain stable operation and prevent damage to the device. For piston devices that do not use dimples or other mechanical means to catch the surface, the collapse of the device typically shorts the opposing plates. As a result, the plates can permanently stick together which prevents any future operation of the device or the device can actually be destroyed by the rush of current through the plates.

This position can be found for both integrated and standard piston devices by modifying Equation (43) letting  $x$  represent the critical deflection such that:

$$\epsilon_o A \kappa V^2 = [t + \kappa(h - x)]^2 2kx \quad (66)$$

where  $V$  is the applied address potential,  $h$  is the resting height of the air gap within the device,  $k$  is the device spring constant,  $\epsilon_o$  is the free space dielectric constant,  $A$  is the area of the opposing plates and  $t$  and  $\kappa$  are the thickness and dielectric constant of the secondary material, respectively. To find the relative maximum of this model, the chain rule is used to determine the differential relationship between the address potential and the critical deflection such that

$$2\epsilon_o A \kappa V dV = -2\kappa[t + \kappa(h - x)](2kx)dx + [t + \kappa(h - x)]^2 (2k)dx \quad (67)$$

which can be algebraically manipulated to solve for the effective derivative of Equation (43) with respect to the critical deflection.

Performing the manipulation and setting the result equal to zero, most of the terms in Equation (67) drop out until the following relationship remains:

$$[t + \kappa(h - x)] - 2\kappa x = 0 \quad (68)$$

which can be solved for  $x$  to reveal an expression for the collapse deflection such that

$$x = \frac{t + \kappa h}{3\kappa} = d_{Snap} \quad (69)$$

where the deflection,  $d_{Snap}$ , is found in terms of the resting height of the air gap,  $h$ , and the thickness of the dielectric material,  $t$ , between the two plates. Any deflection beyond this point will result in collapse of the surface.

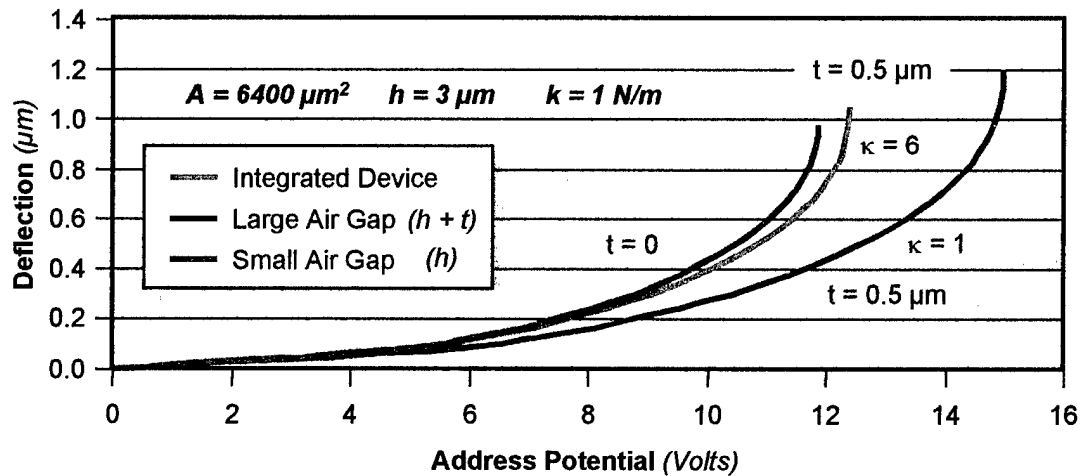
Additionally, the solution in Equation (69) can be used to find the same collapse deflection of standard piston devices. As the thickness of the dielectric material approaches zero, the device behaves more like a standard piston device. Therefore, the collapse deflection of a standard device is found using  $t = 0$  such that

$$d_{Snap} = \frac{h}{3} \quad (70)$$

which indicates that a standard piston device can only demonstrate stable deflections within the first third of the original resting height of the surface.



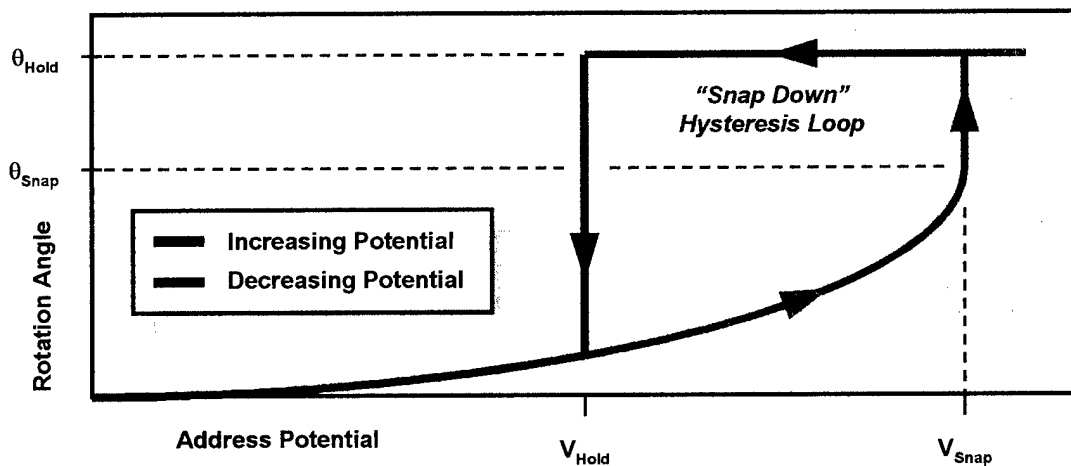
Without special features built within the device to provide a stable landing platform, the device will not be able to maintain a position below this point. As a result, the behavior of such devices is typically plotted only for the stable region of operation. Figure 5-12 illustrates the behavior of such devices by plotting the address potential in Equation (43) versus the desired deflection of the surface.



**Figure 5-12.** Plot of typical behavior of standard and integrated piston devices.

From the curves shown in Figure 5-12, it is easy to see that the device with the largest air gap can sustain the greatest deflection. However, that device requires the largest address potential to actuate to a desired deflection. The curve showing the integrated device and that showing the large air gap device represent the same total distance between plates. From these curves, it is easy to see the effect of the dielectric material above the address electrode. Although the total gap is the same, the integrated address potential is significantly lower due to the increased intensity of the electric field through the dielectric material. The address potential along this curve is almost as low as the device with a much smaller gap consisting only of air.

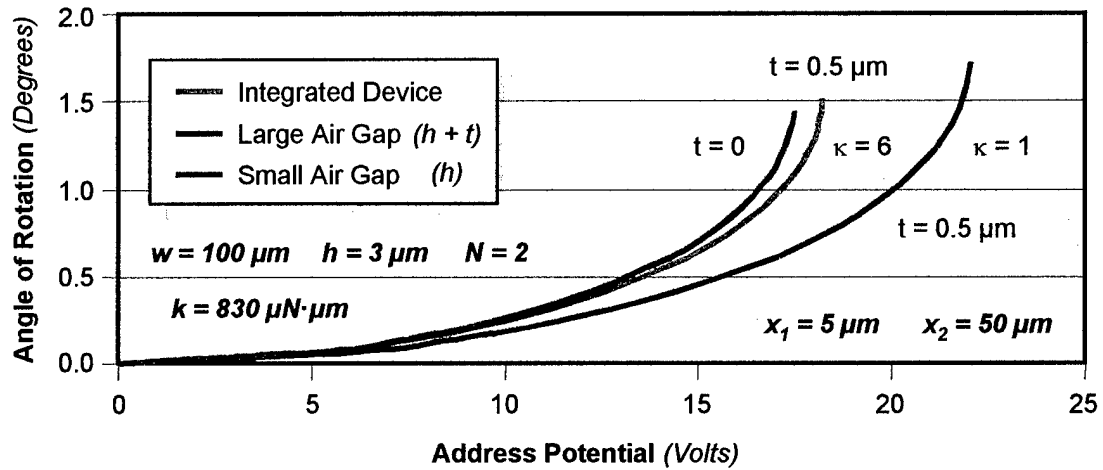
Similar to piston devices, torsion devices have a limited range of stable angles of rotation before collapsing as a result of the same electrostatic capture. For many torsion devices, however, a stable landing pad is designed to catch the surface so that the device is capable of digital or “bi-stable” operation. Such a device is ideal for many optical switching applications in which a channel is to be switched on or off. Figure 5-13 illustrates the general behavior of such a torsion device.



**Figure 5-13.** Plot of typical torsion device surface rotation versus address potential.

As the applied address potential increases, the surface rotates through larger and larger stable angles of rotation. However, once some critical potential has been applied,  $V_{Snap}$ , the surface immediately rotates from the maximum stable angle,  $\theta_{Snap}$ , to the maximum deflected angle,  $\theta_{Hold}$ , which is determined by the landing features built within the device. At this position, the electrostatic force acting on the surface will become much greater since the gap between the plates is minimized. As illustrated in Figure 5-13, a hysteresis loop is created in the device behavior in which a much lower voltage,  $V_{Hold}$ , is all that is required to maintain this position.

For integrated devices, the angle maximizing address potential is also the angle at which the device will collapse as the exponential electrostatic force overtakes the linear torsion spring force [14]. The height and dielectric constant of the oxide layer significantly impact the address potential required to activate integrated devices. Figure 5-14 illustrates the typical behavior of such devices.



**Figure 5-14.** Plot of typical behavior of standard and integrated torsion devices.

As evident in Figure 5-14, the integrated device snaps down at a much lower address potential than a standard device with the same total gap consisting only of air. In fact, the integrated device requires only slightly greater address potential than a standard device with only the same air gap. As a result, standard devices can be bonded onto CMOS receiving chips with very little change in device behavior.

Each of the devices in the Figure 5-14 can reach a maximum stable angle of rotation,  $\theta_{Snap}$ , that increases as the total gap between the surface and the electrode increases. Beyond this angle, various landing features can be designed to hold the surface of the device in a stable position with as much as 20° of tilt angle.

### 5.5.1 Limits of Stable Variable Capacitors

Also evident in Figure 5-12 is the fact that each device can reach a distinct maximum deflection that is roughly one-third of the original resting height of the device. For variable capacitors, this means that a piston device can only achieve a fixed range of stable values. For instance, if the capacitance of an integrated device is determined at rest,  $C_{Rest}$ , and at the maximum stable deflection,  $C_{Max}$ , the total relative change in capacitance of the device is given as

$$C_{Max} = \frac{\kappa \epsilon_o A}{t + \kappa(h - d_{Snap})} = \frac{\kappa \epsilon_o A}{t + \kappa h - \frac{1}{3}(t + \kappa h)} = \frac{\kappa \epsilon_o A}{\frac{2}{3}(t + \kappa h)} = \frac{3}{2} C_{Rest} \quad (71)$$

using Equations (40) and (69) for both integrated and standard piston devices. This indicates that the maximum increase that can be attained by a stable piston variable capacitor is only 50% more than the resting capacitance. As a result, such a device is likely to be rejected for projects requiring a larger range in variable capacitance.

### 5.5.2 Cascaded Collapsing Plate Variable Capacitors

As an alternative, a variety of variable capacitors have been designed with a large number of small plates that are intentionally designed to collapse at different address potentials. Each plate has a distinct spring constant so that only one plate snaps down at a time while the address potential is increased. All plates of the device are designed to rest at the same height above a shared address electrode, but each

plate will achieve a distinct stable deflection provided the address potential is not sufficient to collapse the surface. Once an individual plate is actuated beyond the limit of stable deflection in Equation (69), that plate will collapse. Further increasing the address potential increases the total capacitance of the device as other surfaces collapse in cascading sequence. The result is a much more significant increase in the total capacitance of the device which is based only on the original resting height and the final collapsed spacing of the surfaces. Such devices are capable of reaching a total capacitance that is many times greater than the resting capacitance.

To calculate the total capacitance of such a device, each plate is considered to form an ideal parallel plate capacitor with the address electrode shared by all surfaces. As the address potential is increased, each surface displaces according to its own restoring spring force. Since the separation between the address electrode and the surface will vary between plates, so will the capacitance of that portion of the device. The total capacitance of a device with  $N$  plates connected in parallel is given by

$$C = \sum_{n=1}^N \frac{\epsilon_o A}{h - d_n} \quad (72)$$

where the distinct gap between the surface of the device and the address electrode is defined from Equation (4) for each plate. Since each plate is designed with unique flexures to achieve a distinct spring constant, the deflection of the plates at some address potential will be distributed such that the plate with the lowest spring constant deflects the most and the plate with the highest spring constant deflects the least.

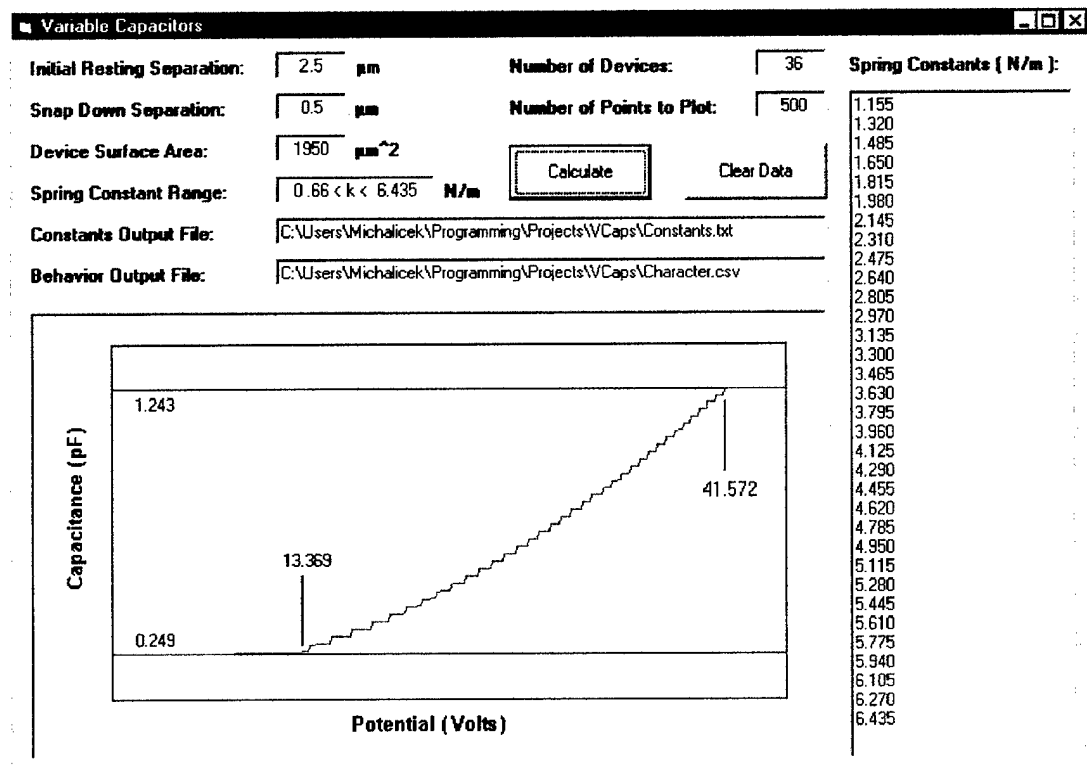
As evident in Equation (72), the total capacitance of the device will be minimized at  $V = 0$  where all plates will rest at the full resting height,  $h$ , above the address electrode. In the resting position, all plates contribute equally to the total capacitance. As the address potential is increased, however, any plates that have collapsed will demonstrate a fixed capacitance that is much greater than surfaces that are still operating in the stable region. Finally, once the address potential is increased beyond the point where the last plate collapses, each plate once again contributes equally to the total device capacitance which is now maximized.

Since it is necessary to treat the address potential of the device as the independent variable, the deflection of each plate must be found by a simple numerical technique in order to calculate the total capacitance. Using Equation (26), the following function,  $f$ , can be defined for a piston device such that

$$f = \varepsilon_o A V^2 - 2k_n d_n (h - d_n)^2 \quad (73)$$

where  $f = 0$  corresponds to the root that solves the model of the piston device. For any applied address potential,  $V$ , the deflection of each plate,  $d_n$ , with distinct spring constant,  $k_n$ , is found numerically by stepping through values of deflection until the root of Equation (73) is found. If that root is greater than the limit of stable deflection given in Equation (69), the surface will collapse and is therefore assigned a fixed separation set by the geometry of the device. The resolution by which the root is determined can be set such that the calculated deflection of the surface is known well within the error induced by the material properties of the device.

To perform this numerical technique as efficiently as possible for a wide variety of devices, a custom software package was written to specifically solve for the capacitance of such a device as a function of address potential. Figure 5-15 shows the primary frame of the variable capacitor calculator showing typical plotted results.



**Figure 5-15.** View of custom software package for variable capacitor calculations.

Although a closed form solution to Equation (72) could be found as a function of address potential for a piston device, such an approach becomes significantly more difficult for other types of devices in which the model is not as simple. In order to accommodate all future devices, the software was designed to use any distribution of spring constants for virtually any electrostatically actuated device.

By comparing the total capacitance of the array of plates in the resting position and in the collapsed position, a total increase in capacitance of the device can be found simply by comparing the initial and final gaps between the plates. Doing so predicts the maximum value of variable capacitance,  $C_{Snap}$ , such that

$$C_{Snap} = \frac{h}{z_{Snap}} C_{Rest} \quad (74)$$

where the  $h$  is the resting height of each plate,  $z_{Snap}$  is the collapsed height of each plate, and  $C_{Rest}$  is the total capacitance of the device at rest. From this equation, it is easy to see that very large ranges of variable capacitance can be achieved by properly designing the resting and collapsed positions of the array of plates forming the device.

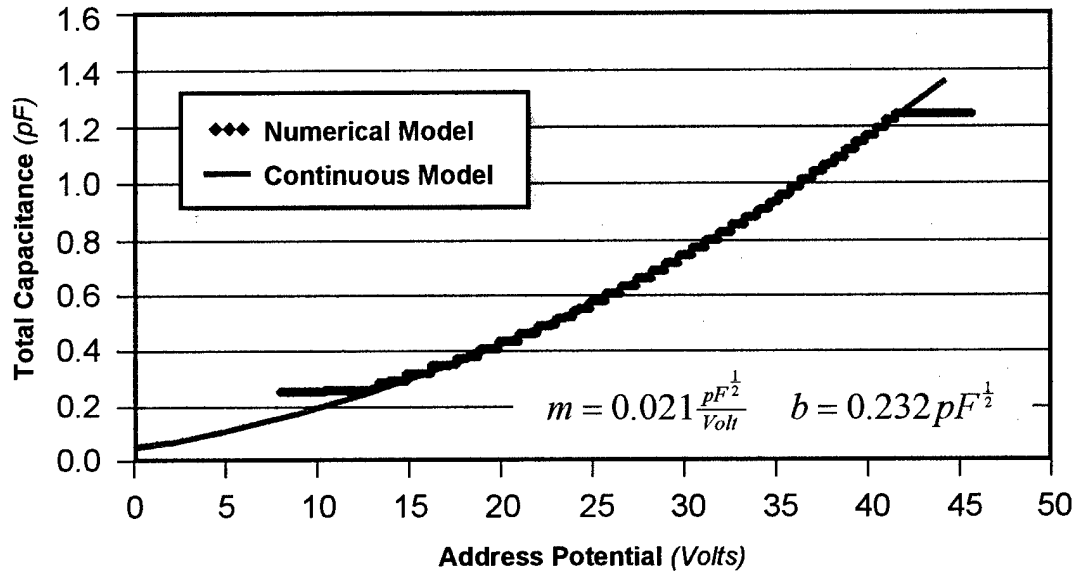
A continuous model can be used to describe the device behavior within the active region between the address potentials where the first and last plates collapse. Essentially, the model can be determined by finding the best-fit line of the square root of the numerical model data. Due to the spring constant distribution, this relationship was known to represent the change in total capacitance as each plate snaps down. The total capacitance of a cascaded collapsing plate device is simply

$$C = (mV + b)^2 \quad (75)$$

which is a function of the applied address potential,  $V$ , and two effective slope and intercept constants,  $m$  and  $b$ , respectively, which are functions of the geometry and material properties of the plates and flexures supporting them.



Using the custom software package, the total capacitance of the device can be evaluated for a range of address potentials. The output file generated by this package was designed to be loaded into a spreadsheet for further analysis. Figure 5-16 shows a plot of such a model as determined by the variable capacitor calculator.



**Figure 5-16.** Plot of a typical behavior curve of a collapsing plate variable capacitor.

The range of total capacitance for the device can be seen in the stepped values as each individual plate collapses. Although the remaining plates are deflecting with increasing address potential, it is the collapse of a single plate that creates the most noticeable effect on the total capacitance. Before the collapse of the first plate, the total capacitance of the device is virtually unchanged. The total capacitance reaches its maximum value after the final plate collapses. At this point, a hysteresis loop is created since much less address potential is required to hold the collapsed plates. As a result, the device must be reset each time a lower capacitance is desired.

## 5.6 Summary

This chapter contains all the necessary tools for developing models and evaluating the behavior of electrostatically actuated devices. Although characteristic models were developed for only a specific set of standard and integrated devices, the definitions and techniques presented herein provide the means by which a model can be formed for virtually any electrostatically actuated device. For instance, the techniques used to develop the model for an integrated torsion device and the standard torsion device with multiple address electrodes can be combined to create a model for an integrated device with multiple levels in the surface of the device. Such designs have been proven to reduce the address potential required to fully deflect the surface of the device. Such considerations are critical when designing devices to operate within the limits of supply voltage of standard CMOS circuits. Ultimately, this chapter should provide an introduction to electrostatic force modeling along with a few examples of proper application.

## **CHAPTER 6**

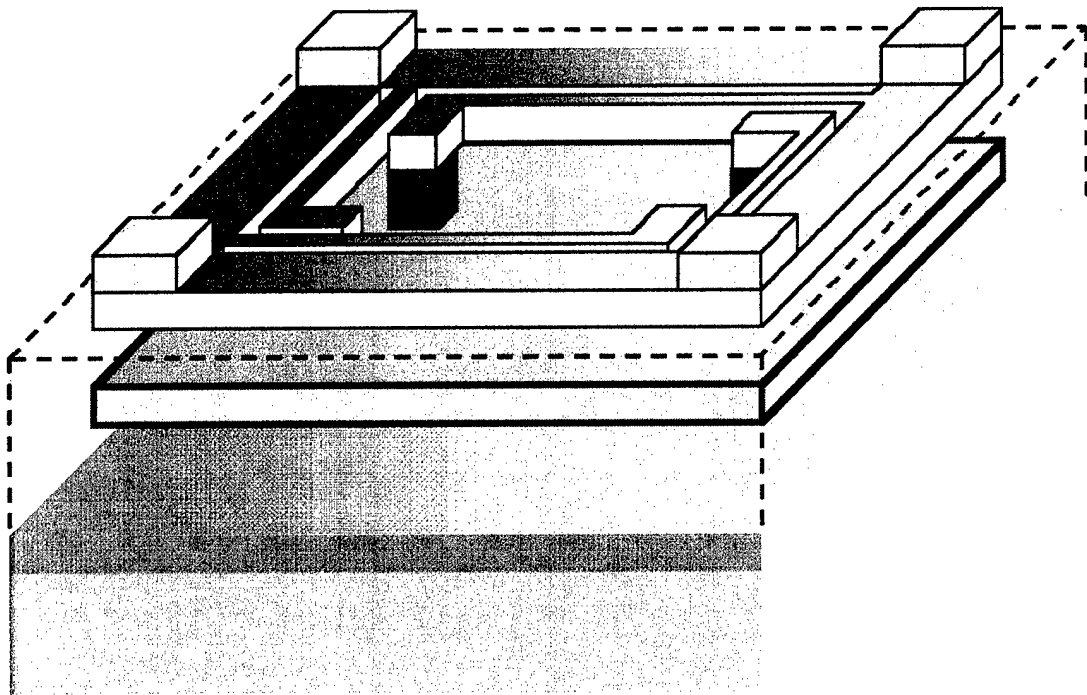
### **FLIP-CHIP ASSEMBLY ONTO CERAMIC SUBSTRATES**

This chapter describes the process by which surface micromachined structures are transferred to ceramic substrates for specific applications that demand the new work surface to support the device. Virtually all devices and procedures reported in this chapter were developed in support of Radio Frequency (RF) applications in which the original silicon substrate typically displays charging effects that prevent the desired operation of the device. The variable capacitors presented in this chapter were flip-chip bonded atop ceramic substrates to prevent the charging effects that would otherwise reduce the signal-to-noise ratio of the circuit below any usable level. The procedures presented in this chapter can be used to transfer virtually any surface-micromachined component onto virtually any other desired work surface.

#### **6.1 Introduction**

The variable capacitor arrays presented in this chapter were fabricated in three phases. First, the surface-micromachined devices were designed and sent for commercial prefabrication. The surface of the device is drawn as the first releasable layer and forms a near perfectly flat plate since no underlying features were patterned

beneath it. This surface is supported only by the sacrificial oxide layer beneath it so that the device is released from the silicon substrate once the oxide is etched from the chip. The device is built upside-down so that the support structure is micromachined above the surface of the device. This support structure also has bond pads patterned in gold. Figure 6-1 illustrates the design of a single piston variable capacitor device.



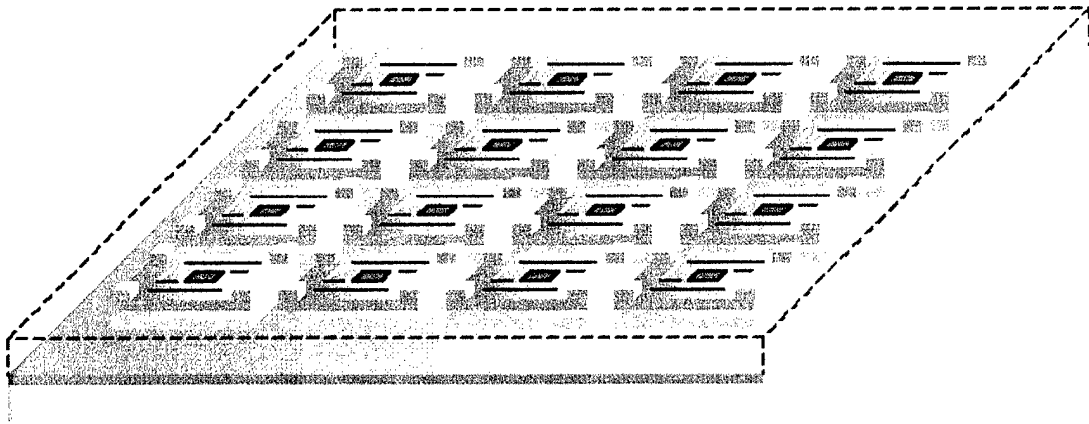
**Figure 6-1.** Illustration of inverted fabrication of a typical piston variable capacitor.

The four gold pads drawn on the support frame are used to make additional electrical contacts with the receiving substrate and as spacers to keep the surface of the device elevated above the address electrodes.

This form of variable capacitor was designed according to well-known design rules and given standard features for such devices. One of two parallel plates was designed to be the moving surface while the other is designed to hold the address

electrode that will actuate it. The surface of the device is supported by four long, thin flexures that will be anchored to the receiving substrate via the support assembly. These flexures provide the restoring spring force that is used to counteract the electrostatic force actuating the device. These flexures varied in design, but were approximately 2-4  $\mu\text{m}$  in width and between 60 and 120  $\mu\text{m}$  in length depending on the specific variable capacitor array. These devices were easily adapted from several previous designs that had proven fully functional.

Once a desired form of the variable capacitor is designed, these devices can be arrayed to achieve any total desired capacitance. Figure 6-2 illustrates an entire array of piston variable capacitors after it is fabricated and delivered from the foundry.



**Figure 6-2.** Illustration of corresponding array of inverted variable capacitors.

The entire array of variable capacitors will remain encased in oxide until the flip-chip assembly is complete at which point the oxide will be removed to free the devices and discard the original silicon host substrate. As described in Chapter 5, each of the devices forms a single element in an array of parallel capacitors. As a

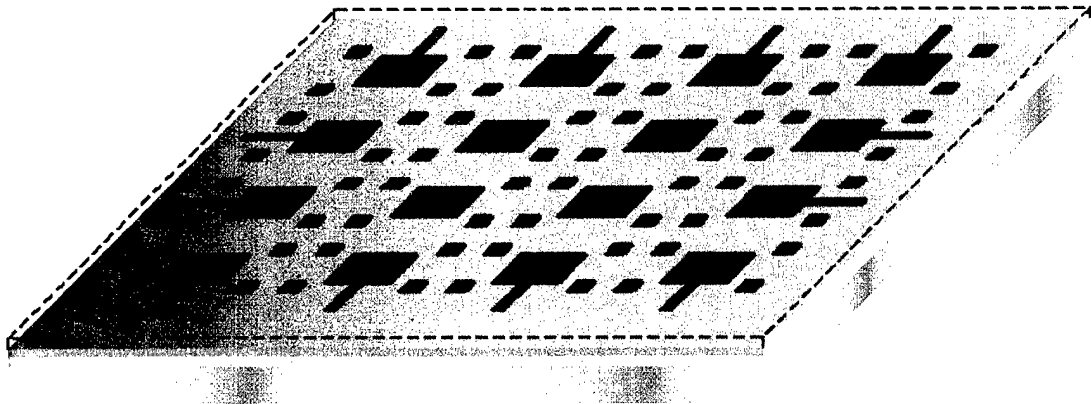
result, numerous devices can be fabricated in large arrays and shorted to the same address lines to form a single large variable capacitor. Each array can be uniquely designed to meet specifications for the desired total capacitance.

Although most of the devices presented in this chapter were designed to comply with the previously determined flip-chip design rules of 30  $\mu\text{m}$  features and spacing, some were intentionally designed to push the limits of the process [10]. Some devices were fabricated with 2  $\mu\text{m}$  features sizes and only 5  $\mu\text{m}$  minimum separation distances between support structures. As a result, many of the flip-chip assembly techniques had to be modified in order to produce working devices and some arrays demonstrated adverse effects due to process variations.

After fabrication, the foundry delivers the 1 cm square chips which contain individual modules designed by several researchers. In order to use a particular chip for flip-chip assembly, it must be diced so that the silicon host module contains only the features intended for flip-chip assembly. Otherwise, the remaining structures may float away during the release etch and contaminate the devices under test. The chips are designed with 100  $\mu\text{m}$  margins between the individual modules to facilitate this process using a standard dicing saw developed for the integrated circuit industry.

The second phase in the flip-chip assembly process is to design and pattern the receiving substrate. For these arrays, a ceramic substrate must be created with gold wires, bond pads, and address electrodes that are exact mirror images of the features of each capacitor array. To create these features, a black-and-white photomask is drawn and printed using a commercial printing shop after which it is used to transfer the pattern observed in the mask to the target substrate.

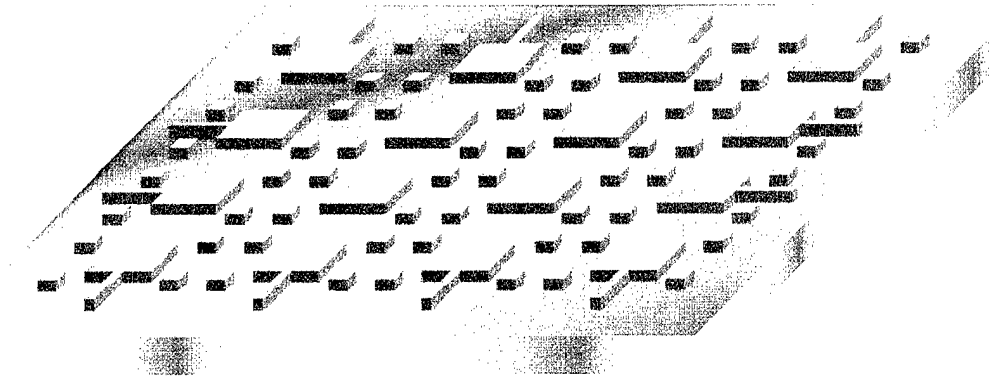
Most of the substrates used in this research were purchased from a commercial vendor with a uniform layer of gold already deposited on the surface. After plasma cleaning this surface, the ceramic substrate is covered with a layer of photoresist. The mask is used to illuminate selected portions of the photoresist and make those portions removable once the photoresist is developed. Figure 6-3 illustrates the placement of the photomask over the uniform layers of photoresist and gold on the surface of the ceramic receiving substrate.



**Figure 6-3.** Illustration of photomask placed atop photoresist over a layer of gold.

Since no features exist on the ceramic substrate, placement of the mask is not critical. The exposed photoresist is irradiated with UV light so that it can be developed much like the film in an ordinary camera. Doing so makes the exposed portion of the material vulnerable to release chemicals that remove the unwanted material yet preserve the portions that were protected under the dark regions of the photomask. This standard photolithographic process is described in greater detail in Chapter 2 in which examples of this etch process are presented using this particular substrate.

Once the photoresist layer is patterned to form the features of the receiving substrate, the gold layer is then etched such that any gold that is not covered by the remaining photoresist is removed. Figure 6-4 shows the resulting ceramic receiving substrate with address electrodes, wires and bond pads patterned on its surface.



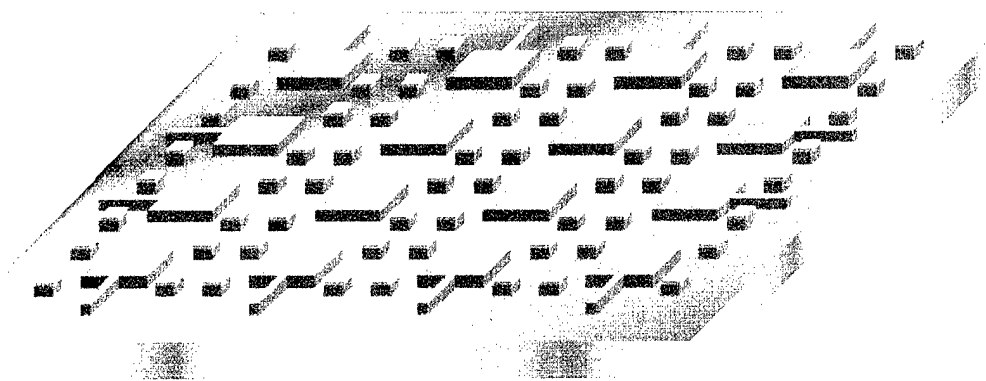
**Figure 6-4.** Illustration of a typical ceramic receiving substrate after gold etch.

In most cases, the gold is used as the address electrodes and to form the address lines that are wired out to probe or wire bond pads. The flip-chip bond pads are formed in gold, but typically require an additional indium layer that is used as an adhesion material between the bond pads of both the host module and the receiving substrate. In flip-chip fabrication that involves direct fusion between the two gold layers, the formation of the ceramic substrate would be complete after the gold etch

The mask pattern used to create the receiving substrate is generated using the layout of the original variable capacitor devices such that the bond pads and address electrodes are the exact mirror images of those originally drawn for the arrays. These features must align perfectly in order to produce fully functional devices.



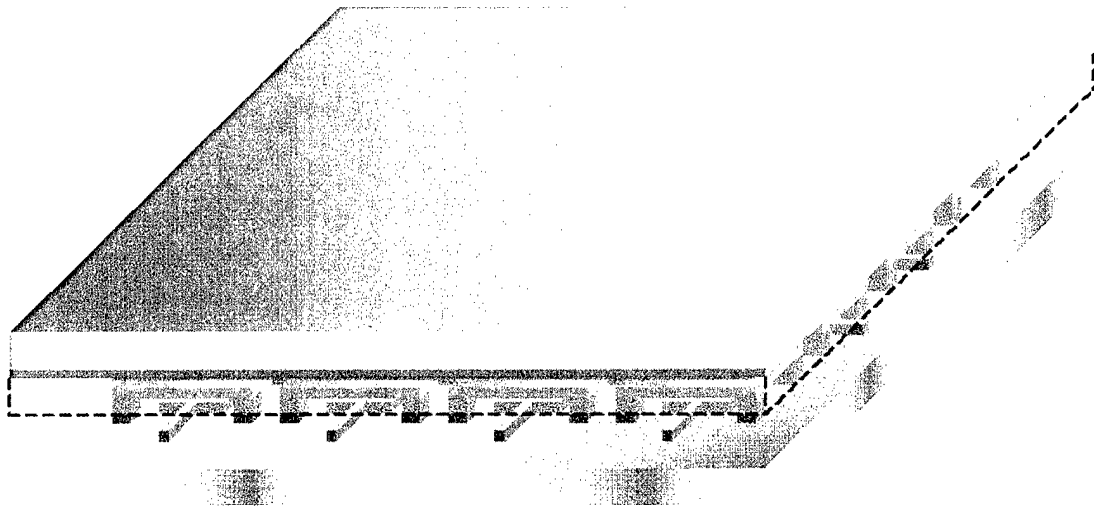
This same mask process is then repeated for a layer of indium which is deposited only on the bond pads. This material acts as an adhesion layer between the gold pads along the support structure of the capacitor arrays and the gold bond pads of the ceramic substrate. A lift-off technique is used to pattern the indium where a layer of photoresist is first added to the ceramic substrate and patterned such that a window is opened above the gold features on which the indium is intended to bond. During indium deposition, it bonds to these features whereas the remaining indium rests atop the layer of photoresist. Removing this photoresist will then free the excess indium which simply floats away. Figure 6-5 shows the final ceramic substrate.



**Figure 6-5.** Illustration of a typical ceramic receiving substrate after preprocessing.

It should be noted that this layer of material and the process by which it is patterned is one of the most significant failure mechanisms of flip-chip assembly onto ceramic substrates. Many of the devices presented in this chapter did not perform as well as expected due to adverse effects of the indium. Primarily, as the indium floats away during the lift-off etch, it tends to accumulate in large pieces on the surface of the devices. Such contamination can damage the device or render it inoperable.

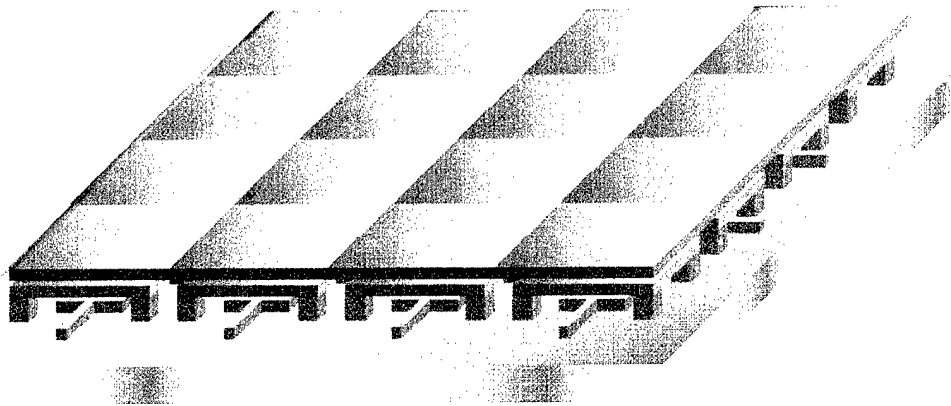
Finally, the surface-micromachined host module and the ceramic receiving substrates are joined using a custom-built flip-chip bonding machine that compresses the opposing bond pads of the two flip-chip modules. With sufficient force and elevated temperature, the indium layer bonds to the gold features and holds the capacitors on the ceramic substrate while still attached to the original silicon host substrate. Figure 6-6 shows the two bonded flip-chip modules.



**Figure 6-6.** Illustration of host substrate bonded atop ceramic receiving substrate.

One of the main concerns during this process is the alignment between the two flip-chip modules. One of the main reasons for the larger design rules used in this process is that the alignment typically demonstrates 10-20  $\mu\text{m}$  of lateral error. In order to improve the results of this process and use devices with much better resolution in the features and separation between adjacent devices, the alignment error must be controlled. As later described, this can be done by design of new features on the modules, a better bonding machine, and better calibration techniques.

After the two modules are bonded together, they are etched in HF to remove the oxide layer that encases the devices and supports the host substrate. During the release, the host silicon substrate is discarded and floats away from the ceramic substrate leaving the arrays behind. Once fully released, the flip-chip devices are rinsed in methanol to displace the acid remaining within the structures. Since the same acids that etch oxide will also etch silicon if given sufficient time, it is important to remove all traces of the acid from within the devices. After several minutes in methanol, the devices are super-critically dried in a special drying chamber that uses liquid CO<sub>2</sub> to displace the methanol. Without this step, the evaporating methanol would pull the arrays into contact with the substrate and destroy most if not all of the devices. Figure 6-7 shows one such array immediately after release and drying.

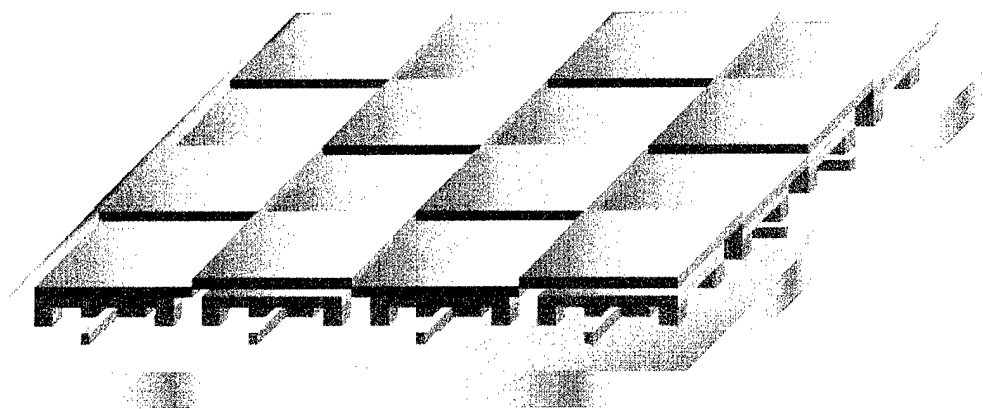


**Figure 6-7.** Illustration of released and dried flip-chip variable capacitor array

The critical point dryer can also be a source of considerable problems when drying these devices. There are typically a number of contaminants within the device so that the mixing of methanol and liquid CO<sub>2</sub> within the chamber redistributes them

across the arrays. Another issue rests in the design of the chamber itself. The mixing of these liquids can be somewhat violent if not carefully controlled by the machine. As a result, some of the receiving substrates flip over so that the arrays make contact with the trays that hold them and a significant number of devices can be lost.

Once the variable capacitor devices are completely released and free to move, they can be tested using a number of techniques. Primarily, a Zygo interferometric microscope is used to measure the deflection of the devices as a function of address potential applied to the address electrodes. As shown in Figure 6-8, doing so actuates the surface of the device so that the capacitance of the entire array increases.



**Figure 6-8.** Illustration of a partially actuated flip-chip variable capacitor array.

For piston type devices, there is a maximum change in capacitance that can be achieved while operating within a stable range of deflections. If the bond pads are designed with sufficient aspect ratio, the indium layer can be deposited to a desired thickness between 1-2  $\mu\text{m}$  in order to customize the array under test. The initial resting height of the array and therefore its initial and maximum capacitance can be designed using the total area of the plates and the stable range of deflection.

### **6.1.1 Background**

This project was originally designed and demonstrated at the University of Colorado as a rapid prototyping technique to develop variable capacitors on ceramic substrates. Although the concept is similar, much of that research was done using large gold balls deposited as the bonding feature [10]. Unfortunately, this does not give very accurate control of the resting height of the devices and therefore the range of attainable values of capacitance. As an alternative, the current technique builds off this background study in order to standardize the deposition of controllable indium layers such that the desired range of capacitance can be achieved by proper design of the area of the arrays and by the thickness of the indium layer.

### **6.1.2 Applications**

As previously discussed, the primary application and the original motivation of this portion of the project was to create variable capacitors for RF circuits. Such devices would be used in highly miniaturized tunable transceivers that require very precise yet highly variable ranges of capacitance in order to adequately adjust the desired filter within the circuit.

This technique could also be used to transfer virtually any MEMS structures to any work surface. For instance, rigid devices can be bonded atop conformal substrates for easy integration with other devices. Surface-micromachined sensors could even be added to systems by “substrateless” bonding directly onto the test structure such as chemical or vibration sensors on lab equipment or vehicles.

### **6.1.3 Advantages**

As previously described in Chapter 3, one of the primary benefits of flip-chip assembly is the inherent planarization of the flip-chip structures. The upper layers of a flip-chip assembled structure are prefabricated on a separate host substrate such that no topographical effects are created in the surface by lower layers. As a result, problems typically associated with mechanical linkages, variable capacitors, and optical components can easily be eliminated by improved design of flip-chip devices.

The other notable advantage of flip-chip assembly is the ability to transfer MEMS structures to virtually any work surface. Although this chapter describes the flip-chip assembly of polysilicon structures atop ceramic substrates, these same procedures can be used to create advanced MEMS components on other substrates. Most flip-chip devices can be transferred to virtually any desired work surface that can be optimized for specific desired material properties such as thermal expansion, thermal conductivity, electrical conductivity, and dielectric properties.

### **6.1.4 Disadvantages**

Probably the most significant disadvantage of this form of flip-chip assembly is the need for highly specialized equipment. The flip-chip assembly technique requires a custom-built, computer-controlled machine to facilitate and regulate the bonding process. Although somewhat similar machines can be purchased for some flip-chip purposes, the equipment used to perform this research was not commercially available and can cost a considerable amount of time and money to build.

The flip-chip bonding machine required for this assembly technique is also the source of another problem common to this process. Without repeated calibrations, the machine can demonstrate significant alignment errors between host and receiving modules that sometimes produce disabled or even inoperable devices. Although this error can be minimized by both design of modules and bonding technique, the ability to bond two features within a required alignment tolerance will always be an issue.

Finally, this form of flip-chip assembly often requires complex preprocessing necessary to prepare a ceramic receiving substrate. From the original design and printing of the gold and indium masks to the final stages of photolithography and lift-off used to form those patterns on the substrate, there are numerous lengthy and costly steps that must be performed before the bonding process can begin. It is not uncommon for the preparation of a ceramic host substrate to take many days while the bonding process itself takes only a few hours.

## **6.2 Implementation**

The flip-chip assembly of polysilicon features onto ceramic substrates consists of three phases of fabrication. First, the prefabrication of the MEMS host module is relatively simple and poses little design risk. Second, the ceramic substrate must be created to receive the host module. Because of the complex preprocessing of ceramic substrates, the bulk of the process difficulty and potential failure rests in this phase of fabrication. Finally, the two must be bonded using the flip-chip bonding machine. This section describes each phase of fabrication in greater detail.

### 6.2.1 General Design Considerations

Before either the MEMS host module or the ceramic receiving substrate are designed, the intended range of capacitance must be determined. The resting and fully actuated capacitance values for these arrays are determined by the total surface area and the initial resting gap of the array. The total area can simply be increased or decreased by adding or removing devices in parallel, respectively. The resting gap of the array can be adjusted by a combination of the layer selection when designing the surface-micromachined capacitors and the thickness of the indium layer used to bond them to the ceramic substrate.

Due to slight bonding variations that are typical when using an indium adhesion layer between bond pads, the actual range of capacitance of an array often varies from the original design. The resting gap across the array is often not as uniform as expected or the alignment between modules is such that the overlap of each pair of plates and therefore the capacitance of each device is less than designed. As a result, a very tight tolerance in the design specifications may create problems when fabricating the devices.

There are two primary types of arrays reported in this chapter. The first uses a common bonding frame surrounding and supporting all devices within the array. This frame consists of four large bond pads in the corners of the arrays that anchor the array to the ceramic substrate. In this manner, the entire array can be successfully transferred to the substrate if only a portion of these pads form a complete bond. On the other hand, variances in the indium layer and alignment errors can create sometimes severe adverse effects within the array that alter the range of capacitance.

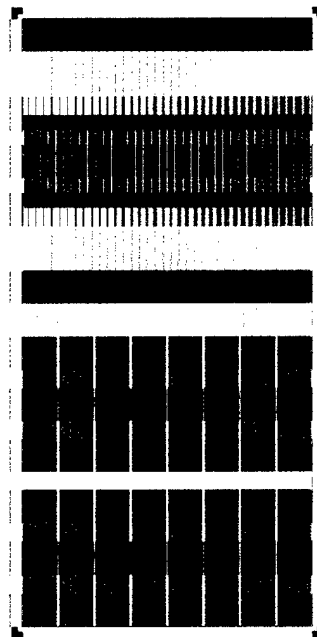


The second type of array is one consisting of individually bonded devices. Each device within the array has four bond pads in the corner of the device so that there is no mechanical connection to any other device within the array. Although each device is more likely to behave as desired, some devices within the arrays simply do not form sufficient bonds with the substrate and float away during the release etch. As a result, neither type of array is ideal for creating a total variable capacitance that is repeatedly and accurately determined by design.

In addition to variances induced by the bonding of these arrays, there is also a fundamental limit in the range of capacitance that can be achieved using piston devices operating in a stable mode. As described in Chapter 5, the capacitance of a piston device can only increase by a maximum of 50% over the resting value before the surface deflects enough to collapse. When combined with the inherent variances due to bonding the arrays, the actual capacitance of the fabricated arrays may not achieve the design value. The total range of variable capacitance of the final array may not fall within the intended range required for the desired application.

The solution to these problems is simply to design the arrays with the ability to tune the total capacitance created by the parallel distribution of piston devices. Although the total increase in capacitance remains only 50% of the resting value, the maximum and minimum values can be calibrated simply by adjusting the total surface area of the array. The arrays can be designed with many more devices than required by the design specifications and then trimmed to the desired actual capacitance by removing individual devices. The total surface area can be experimentally tuned to achieve the desired resting and therefore maximum value of capacitance.

Taking this improvement one step further is a new type of variable capacitor that breaks the limit of maximum capacitance set by stable piston devices. The arrays shown in Figure 6-9 consist of a set of plates supported by flexures that vary in width and therefore the spring constant of each plate. As a result, each plate will collapse at a distinct address potential and, in doing so, will increase the capacitance of the array.



**Figure 6-9.** Illustration of a cascaded collapsing plate variable capacitor design.

This cascaded collapsing plate device allows for a significantly increased range of variable capacitance since the capacitance of each individual plate changes more significantly than a stable piston device. To prevent shorting when the device collapses, a variety of simple mechanical features can be employed to stop the surface of the device before it makes contact with the address electrode beneath it. In setting this collapsed gap, a stable maximum capacitance can be attained.

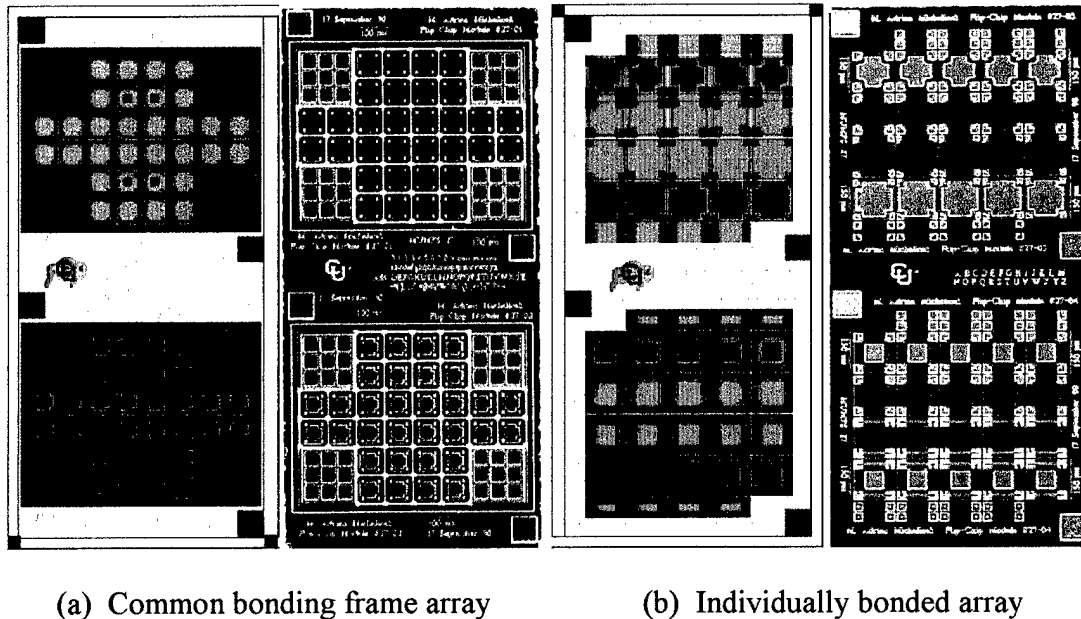
As described in Chapter 5, the maximum and minimum capacitances are only a function of the collapsed and resting gap between the plates, respectively. The larger gaps between the resting plates produce some nominal resting capacitance that is the minimum value attainable by the array. As the address potential is increased, each plate collapses in sequence and increases the total capacitance in small increments. If the collapsed gap is designed to be very small compared to the resting gap, the maximum capacitance can be many times greater than the resting value. The result is a much greater range of variable capacitance.

As previously described, it is difficult to accurately predict the nominal capacitance of the array due to variances in bonding the devices to the ceramic substrate. Again, fixed capacitors wired in parallel to the collapsing plates can be used to tune the finished array. As shown in the lower portion of Figure 6-9, a set of such devices can be bonded along with the variable capacitor array to adjust the values of capacitance attainable by the collapsing plates. These devices are designed to be removed individually until the desired nominal capacitance is obtained. Likewise, the indium mask can be easily adjusted in order to select the number of fixed devices that bond to the substrate. The rest simply float away during release.

One of the more important design aspects of these devices is the address potential limit at which a collapsed plate will deform and short with the address electrode. The first plate to collapse may short before some of the higher-voltage plates even collapse. For added flexibility, the variable capacitor array in Figure 6-9 is segmented into blocks of six plates that share a pair of bond pads so that either end of the array can be similarly trimmed to prevent such a failure of the entire array.

## 6.2.2 Prefabrication of MEMS Host Module

The polysilicon variable capacitor arrays were designed for fabrication in the MUMPS service such that the uppermost material is a gold layer used in the bonding process. The first array designs used four large bond pads anchored to a common bonding frame while others had individually anchored devices. Figure 6-10 shows the initial layout and resulting diced flip-chip module for both types of array designs.



**Figure 6-10.** Layouts and photographs of flip-chip piston variable capacitor arrays.

The larger bond pads shown in Figure 6-10(a) support the devices by a common bonding frame that is also used as a ground plane during actuation. This design proved to be less effective than others as internal thermal stress between gold and polysilicon layers and slight misalignments in the bond pads create a noticeable stress and resulting deformation across the surface of the array.

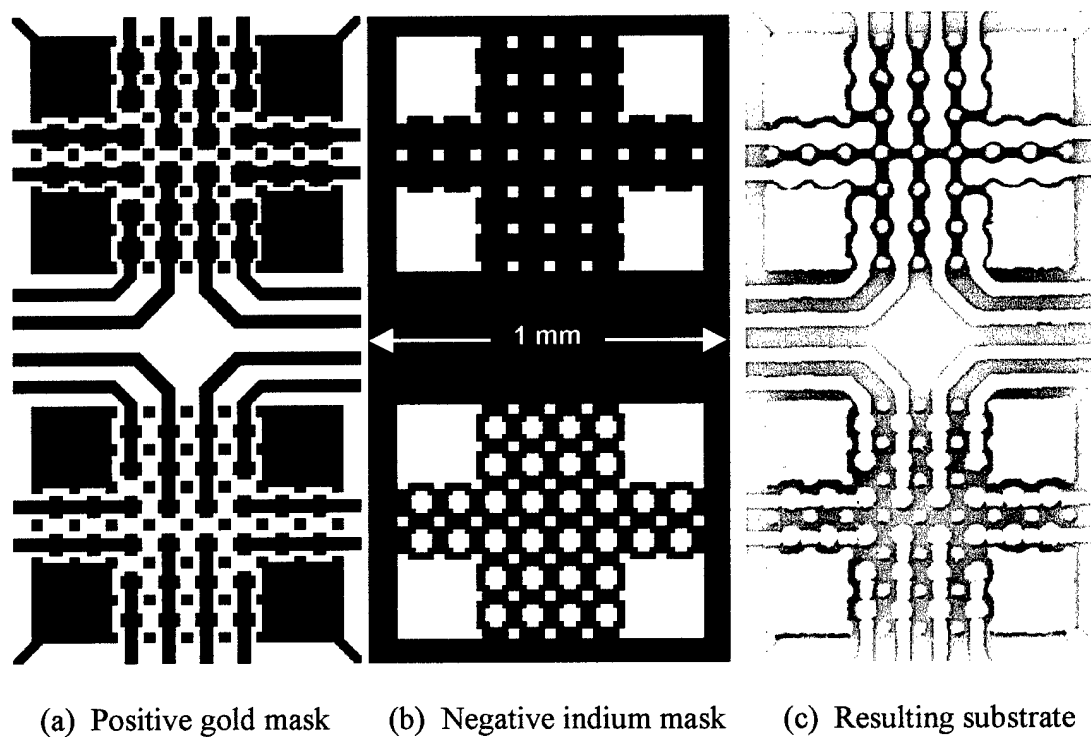
The squares shown along the edges of the 1 x 2 mm modules are used for alignment of the dicing saw used to separate the individual modules. Figure 6-10(b) shows two arrays of individually bonded variable capacitors. The devices shown in Figure 6-10(a) are 100  $\mu\text{m}$  square while the devices in Figure 6-10(b) are 150  $\mu\text{m}$  square. These devices were enlarged in order to accommodate the area needed to form the individual bond pads within each device.

The four large bond pads shown in Figure 6-10(a) were the very first attempt to bond such arrays to the ceramic substrates. They would eventually prove sufficient for variable capacitors or other electrical devices, but ineffective for supporting micromirrors or other devices in which array planarity is an issue. The individually anchored devices shown in Figure 6-10(b) were better suited to more planarized arrays, but pushed the bonding limits of the process. The smaller size of the bond pads within each device reduced the bonding yield since some devices did not completely bond and floated away with the substrate during the release etch.

As shown in Figure 6-10, some of the devices within either type of array are designed with elevated address electrodes to reduce the address potential required to actuate the device. These electrodes are prefabricated on the host module and then transferred to the receiving substrate to reduce the resting gap between the plates of the device. The chips were successfully diced while the chips were still encased in oxide and a protective layer of photoresist so that the rough vibrations during dicing do not damage or destroy the arrays. After dicing, the photoresist is removed from the chips to expose the gold bonding pads for processing.

### 6.2.3 Preprocessing of Ceramic Receiving Substrate

One of the most difficult and tedious tasks in preparing flip-chip modules for bonding on ceramic substrates is the preparation of the substrate itself. The features patterned in gold and the layer of indium used to bond them require a considerable amount of processing to achieve. For both layers, a photomask must be drawn, printed, and transferred to glass before the features of each layer can be patterned using a standard photolithographic process. The general concept is illustrated in Figure 6-11 which shows both mask patterns and the resulting ceramic substrate.



**Figure 6-11.** Illustration of masks and resulting features on a ceramic substrate.

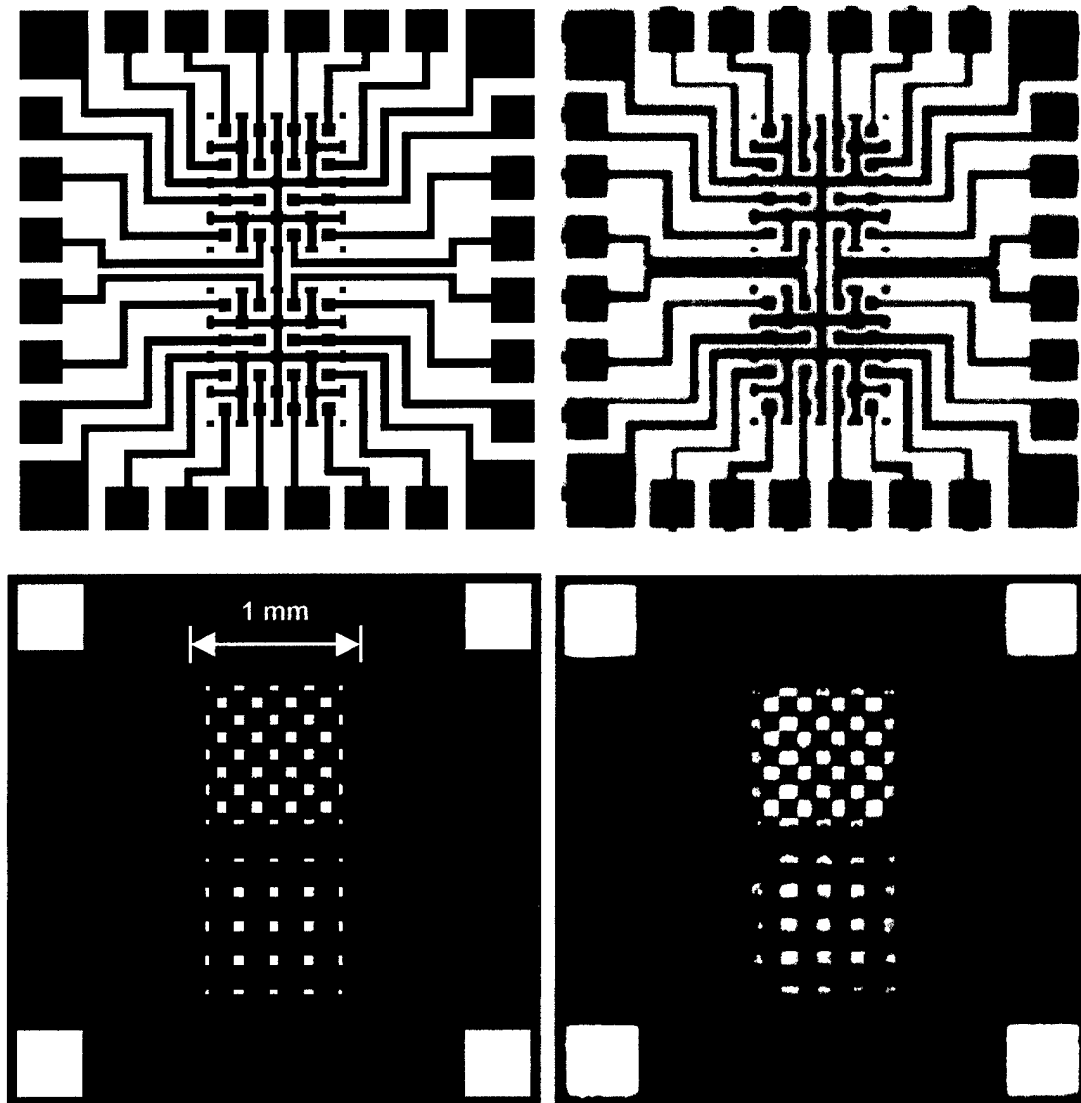
The positive gold mask is used to define the address electrodes, wiring, and bond pads on the ceramic substrate. As illustrated in Figure 6-11(a), the dark regions of the

mask determine the features of the final gold regions. The negative indium mask is used to define the bond pads using a lift-off process described in Chapter 2. Due to the nature of this deposition process, the light regions of the mask in Figure 6-11(b) will determine the regions of indium on the ceramic substrate. Figure 6-11(c) shows the resulting ceramic substrate after both masks were processed independently. The large indium regions in the corners of the receiving substrate correspond to matching gold bond pads on the host module that are connected to the variable capacitor arrays. The indium patterned on the address wiring in the lower half of the substrate is intended to receive address electrodes that were designed as part of the variable capacitor on the host module. The devices intended for bonding on the upper half of the substrate were designed without a self-contained address electrode.

One of the drawbacks of this approach to flip-chip assembly is the maximum resolution at which the masks can be printed and the minimum feature size that can be realized in the finished substrate. The gold mask shown in Figure 6-11(a) and the indium mask shown in Figure 6-11(b) were drawn with minimum feature and spacing sizes of 10  $\mu\text{m}$  which significantly pushed the limits of the process. Based on the existing technique at the time these substrates were made, each mask should have been drawn with 30  $\mu\text{m}$  features to ensure that all patterns were safely defined. Many substrates, like that shown in Figure 6-11(c), had to be overetched to prevent shorting between wires. As a result, many of the gold features that were drawn in rectangular or "Manhattan" shapes appear rounded and reduced in size on the final substrate.

Additionally, in order to accommodate the needs of some printing shops, the files containing the mask data had to be stored in postscript form. Due to the nature

of this file type, many of the features were rounded to a common file factor such that much of the required resolution was lost. Figure 6-12 shows the effect of this error.



(a) Original gold and indium layouts

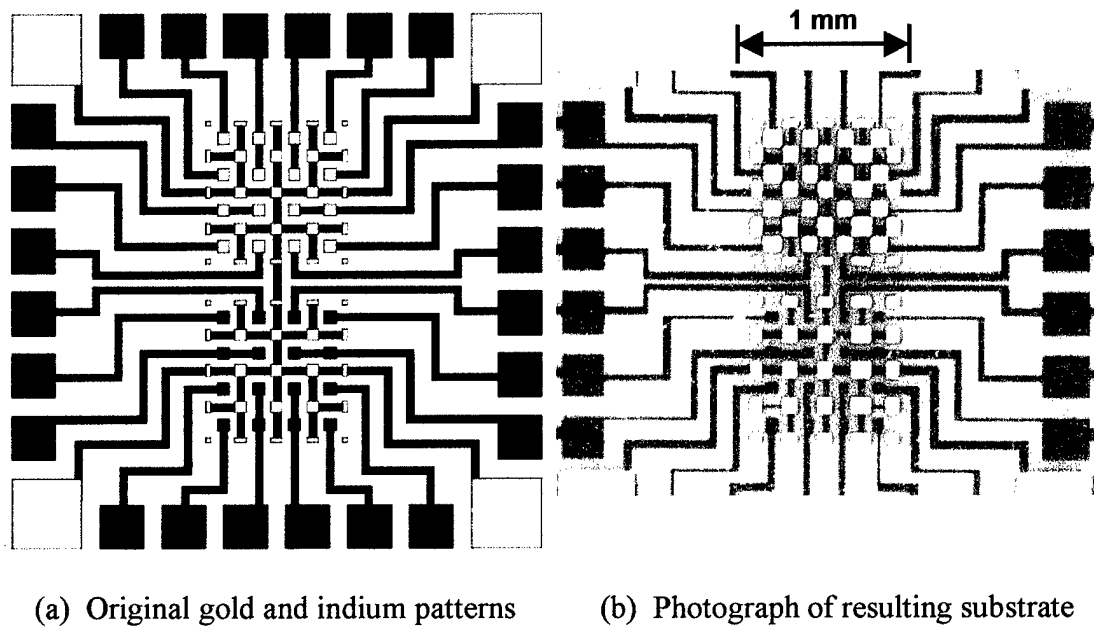
(b) Photograph of resulting masks

**Figure 6-12.** Illustration of postscript file rounding errors evident in mask features.

Both the original gold and indium masks layouts in Figure 6-12(a) illustrate uniformly shaped and spaced features that were intended to be realized on the



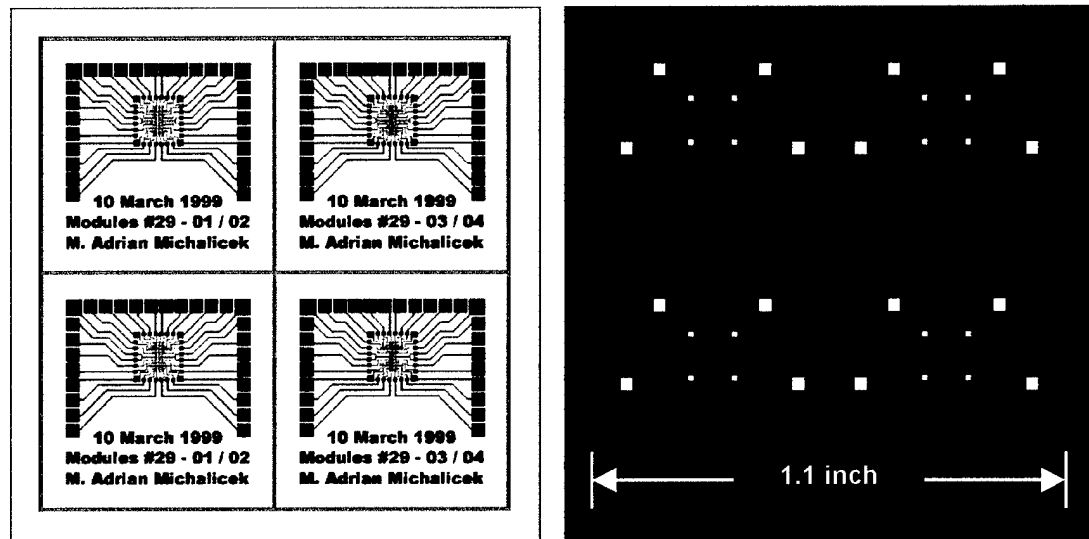
ceramic substrate. As shown in Figure 6-12(b), however, the resulting masks display odd shapes and spacing between features. The rounding error is such that positive features of the masks often appear smaller or slightly shifted in position. As a result, the negative areas used for the indium deposition may also appear slightly enlarged. Figure 6-13 illustrates the final effect of such rounding errors in the mask files.



**Figure 6-13.** Illustration of common rounding errors associated with printed masks.

As shown in Figure 6-13(a), the combined gold and indium features should be very uniformly spaced and separated from other features patterned with the same mask. As evident in Figure 6-13(b), however, the resulting features are distorted and many of the indium pads over address electrodes within the arrays are shorted with ground line pads which renders that device useless. In this manner, the pursuit of additional printer resolution was a moderate failure. Other attempts using lossless file types such as TIFF or GIF formats have proven to mostly preserve the intended pattern.

In general, each of the 1.1 inch square ceramic substrates was patterned to hold test structures from several flip-chip host modules. Each was designed so that these areas could be diced into smaller substrates for future testing if the need existed. Figure 6-14 shows the layout of a typical gold mask and the corresponding indium mask used to create such a substrate.



(a) Typical positive gold pattern

(b) Typical negative indium pattern

**Figure 6-14.** Illustration of full-size gold and indium masks for ceramic substrates.

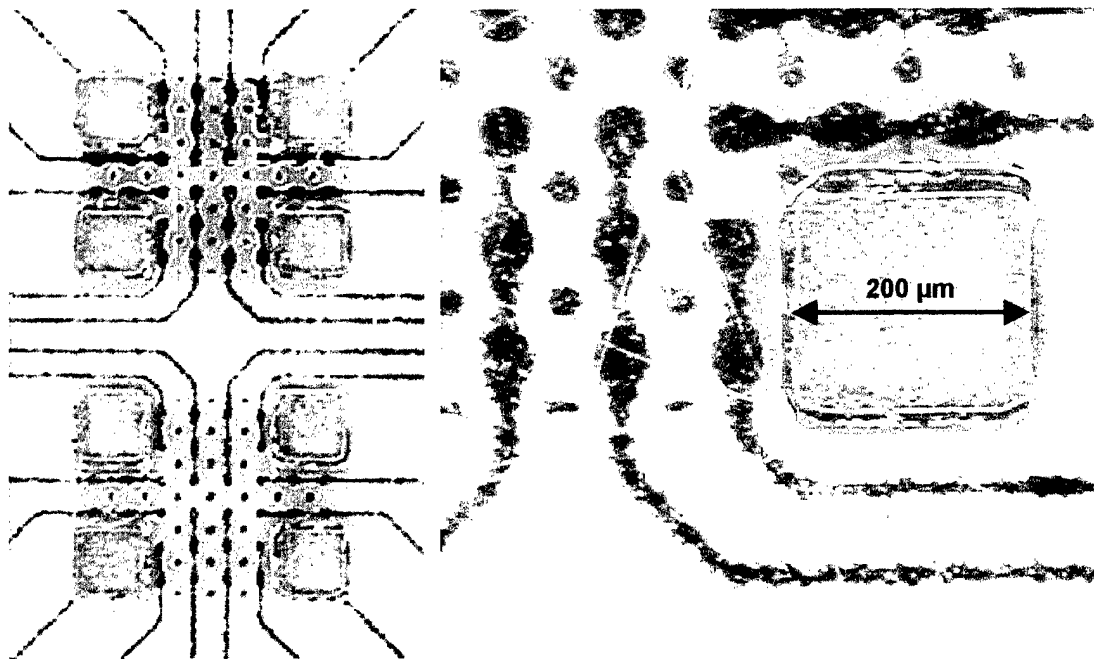
The outer edge of the positive gold mask layout in Figure 6-14(a) is simply a border designed to maintain accurate sizing with the indium mask. None of the outlines in this layout correspond to actual gold features. It is important that the two masks be drawn with the same absolute size such that any modification to one during the printing process will likely have the same effect on the other. The indium mask shown in Figure 6-14(b) is drawn larger than the actual substrate so that no remnant lines of indium remain around the edge of the substrate following the lift-off process.

The bond pads and address electrodes for two variable capacitor arrays are placed in the center of each quadrant shown in Figure 6-14(a) such that a ring of probe pads is wired to each row of devices followed by wire bonding pads connected to the same line. The corresponding indium masks in Figure 6-14(b) are drawn with large openings that fit over several gold probe and wire bonding pads on the substrate for alignment purposes. These gold pads are redundant ground lines that do not require probing or other electrical connections. For size comparison, the receiving areas for two arrays shown in Figure 6-11 are placed in the center of the probe pad ring shown in Figure 6-12 and Figure 6-13 which is in turn placed in the center of each substrate quadrant illustrated in Figure 6-14. In this manner, this particular substrate is designed to receive a total of eight distinct variable capacitor arrays.

Similar to the gold mask, the corresponding bond pads used to anchor the arrays to the substrate are placed in the center of the quadrants in the indium mask. The address wiring and bond pad layouts for both masks are generated from the original device layout such that the patterns are simply copied as mirror images of the device pads. Additionally, many of the variable capacitors arrays designed for ceramic substrates were drawn with very symmetrically distributed bond pads within the arrays. Both techniques tend to reduce various errors when assembling the devices since any small variance between masks can render some devices unusable.

The same procedure was performed for the deposition of indium as an adhesive layer between the gold layer on the substrate and the gold on the bond pads of the variable capacitor arrays. The excess indium is removed by a process of lift-off where a thick layer of photoresist is deposited on the substrate and patterned with the

indium mask prior to the deposition of the indium. The light areas of the indium mask open a hole in the photoresist to expose the desired gold of the bond pads beneath it. Ideally, only portions of the indium layer that bond to the gold pads will remain after the photoresist is removed since the excess indium will float away. Figure 6-15 shows a typical pattern of indium after the deposition of a 1.8  $\mu\text{m}$  indium adhesion layer on the four large bond pads of the common bonding frame array.



(a) Photograph of receiving area

(b) Photograph of individual bond pad

**Figure 6-15.** View of one processed receiving area of a typical ceramic substrate.

The rough edges of this process can be seen in Figure 6-15(b) where the edges of the pad were sloped upward to conform to the pattern of the photoresist upon which the excess material was deposited. Many of these edges contribute to the excess indium contamination that was later observed in a large number of these arrays.

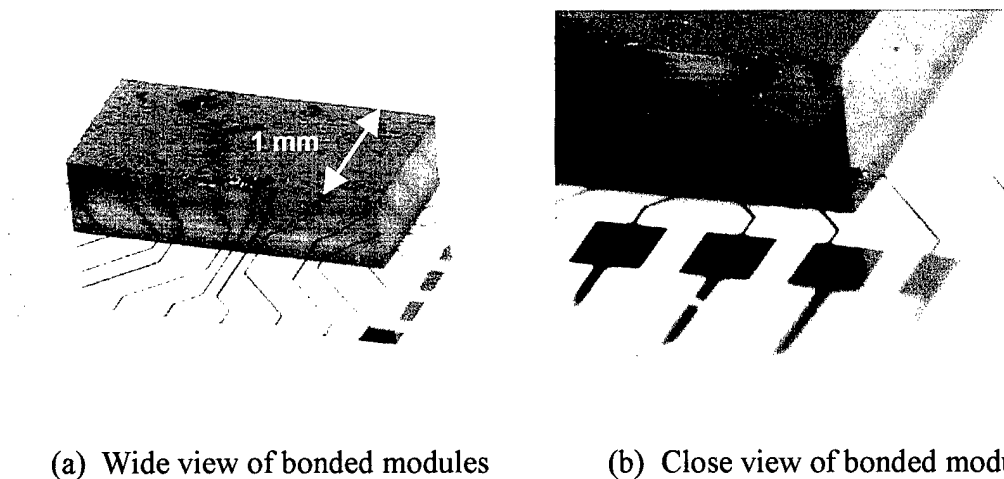
The effects of overetching the gold wiring can be seen where the wiring, address electrodes, and bond pads are distorted around the edges and appear jagged and hazy rather than smooth and reflective as the gold layer originated. Such overetching attacks the gold that is required to bond and actuate the devices and is potentially devastating to the process since address wires can be totally removed.

Additionally, the address potential required to actuate the devices can be significantly higher than expected as a result of the overetching. First, the rounded edges of the bonding pads created a noticeable error in alignment when the modules are bonded to the ceramic substrates. This misalignment can position each address electrode off center beneath the surface of the device and therefore create a moderate loss in electrostatic force during actuation. Likewise, the reduction in surface area of the address electrodes means that a much higher potential must be applied to achieve the same electrostatic force as a larger and better defined electrode.

#### **6.2.4 Assembly of Flip-Chip Modules**

The flip-chip assembly of the variable capacitor arrays was first performed on the original flip-chip bonding machine. This machine was custom-built at the University of Colorado and enables both thermocompressive and thermosonic bonding of gold and indium features. Although the original machine had previously demonstrated capabilities that were sufficient for larger scale bonding applications, many of the variable capacitor arrays displayed adverse bonding characteristics that were in some way induced by alignment error inherent to this machine. Many of these conditions were reduced once the new bonding machine had been completed.

Once the substrate and host module are prepared, the flip-chip bonding machine is used to bond the arrays to the receiving substrate. The bonding machine allows for precise tip, tilt, and rotation alignment similar to a common mask aligner used in photolithography. Once aligned, the chips are pressed together under high force and temperature so that the indium layer bonds to the two gold layers and forms the structural bond between the devices and the ceramic substrate. Figure 6-16 shows the bonded module atop the ceramic substrate after this step in the assembly process.



**Figure 6-16.** Photographs of a typical host module bonded atop a ceramic substrate.

The bonding of the host modules was typically quite successful, producing numerous complete arrays of devices fastened to the ceramic substrate. During this process, however, a significant amount of force was required to overcome the effects of overetching the gold where there was less surface area available for bonding. As a result, the arrays often showed a moderate alignment error after shifting during the bonding phase as the indium layer became more compliant at higher temperature.

Once bonded and cooled, the indium forms a strong bond sufficient to support the silicon substrate only by the bond pads of the variable capacitor arrays.

As shown in Figure 6-16(b), the cuts made from the dicing saw are clearly visible along the side of the silicon host substrate and a small gap can be seen between it and the ceramic receiving substrate. This gap is the only means by which the HF can reach the oxide that encases the devices and supports the silicon chip on the ceramic substrate. As a result, a slightly longer release etch was anticipated compared to that required for the normal release of surface-micromachined devices.

Once bonded, the modules are rinsed in HF to etch the oxide and free the silicon host substrate from the arrays that are bonded to the ceramic substrate. The release etch must penetrate the entire width of the chip and will require more time and some agitation to accomplish the release. However, if the device is allowed to rinse in the acid for too long, the polysilicon features of the devices may begin to etch as well. Therefore, the entire acid rinse was stirred and agitated in a circular motion to pass as much acid through the gap between the chips as possible while minimizing the time spent in the acid. After approximately 7-10 minutes, the silicon chips fall off the ceramic substrates leaving the variable capacitor arrays behind.

In some cases, the agitation was sufficient to damage some of the devices within the arrays. As the last of the oxide was being removed, the underside of the surface was released before the silicon chip released the same surface from above. As a result, the flexures of a few devices within the array are left to support the load of the entire silicon host substrate via the oxide column connected to the surface. During agitation, the motion of the acid pushed the chip with sufficient force to pull

the device from the array and leave only the support structure in its place. The formation of oxide columns is discussed in greater detail in the following chapter.

Immediately after the release etch, the ceramic substrates with the attached arrays are rinsed in methanol to displace the acid from beneath the devices. After a sufficient rinse in methanol, a super-critical CO<sub>2</sub> drier is used to displace the methanol with liquid CO<sub>2</sub> which is then heated and pressurized until it super-critically evaporates with little or no surface tension to damage the devices. After drying, the released arrays are examined to determine whether the assembly process produced working devices. Figure 6-17 shows a typical released array of variable capacitors.



**Figure 6-17.** Photograph of common bonding frame arrays on a ceramic substrate.

The only device that failed during the assembly process is one along the edge of the array at right. This device was damaged during the release etch by the formation of an oxide column which eventually pulled the surface of the device from the array.

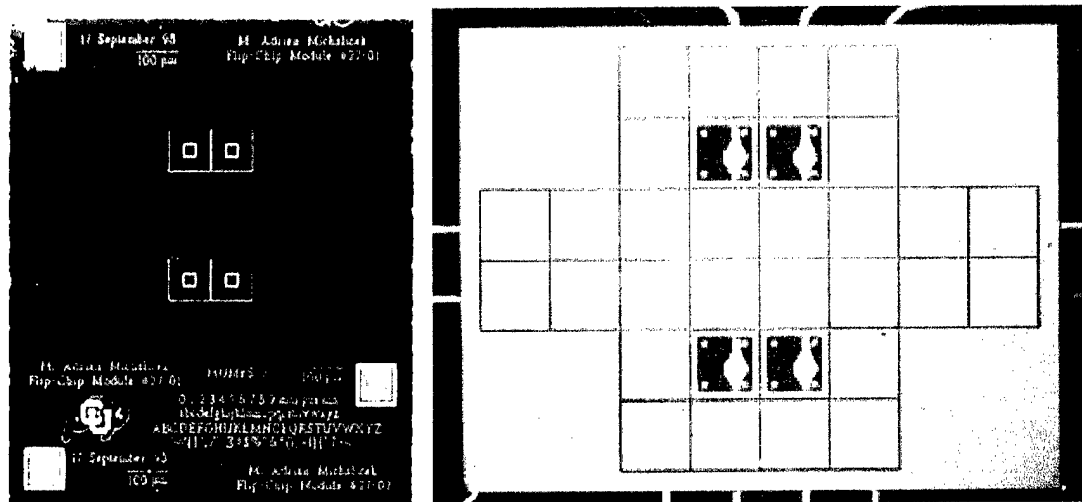


The devices shown in Figure 6-17 are supported by a common bonding frame that is anchored to the ceramic substrate by four large bond pads in the corners of the arrays. Although this bonding frame simplifies the assembly of these devices, it poses additional problems that may limit or prohibit the operation of other flip-chip devices. As described in the following sections, these bond pads produce a stress across the surface of the array that can severely obstruct its intended performance. As a result, more demanding devices such as micromirrors or other optical components may be rendered useless if the entire surface of the arrays is not perfectly planar.

One of the main problems with this type of flip-chip bonding is also evident in Figure 6-17 in which several large particles of indium can be seen on the surface of the array. This type of contamination is fairly common with ceramic substrate bonding in which the layer is typically used for adhesion between the bond pads of the two opposing modules. Unfortunately, the lift-off process by which the layer is patterned is not ideal and small traces of indium remain distributed across the surface of the substrate. As a result, these remnant layers of indium tend to accumulate during the release etch and manifest in large fragments on the flip-chip structures.

Also visible in Figure 6-17 is another effect of overetching the gold patterns to accommodate tighter features within the array. The address wires running from the ring of probe pads surrounding the arrays can sometimes delaminate from the surface of the ceramic substrate such that the wires are left floating along its surface. Many of these wires are long enough to interfere with other address lines or simply break during release or other handling of the ceramic substrate. In some cases, these wires burn out like fuses during actuation of the devices even at low address potentials.

The alignment error that was common with early flip-chip bonding onto ceramic substrates can be seen in Figure 6-18(b) in which several address electrodes are exposed beneath the surface of the entire array. These electrodes are visible through the openings that were created when the surfaces of these devices were removed along with the host substrate during the release etch.



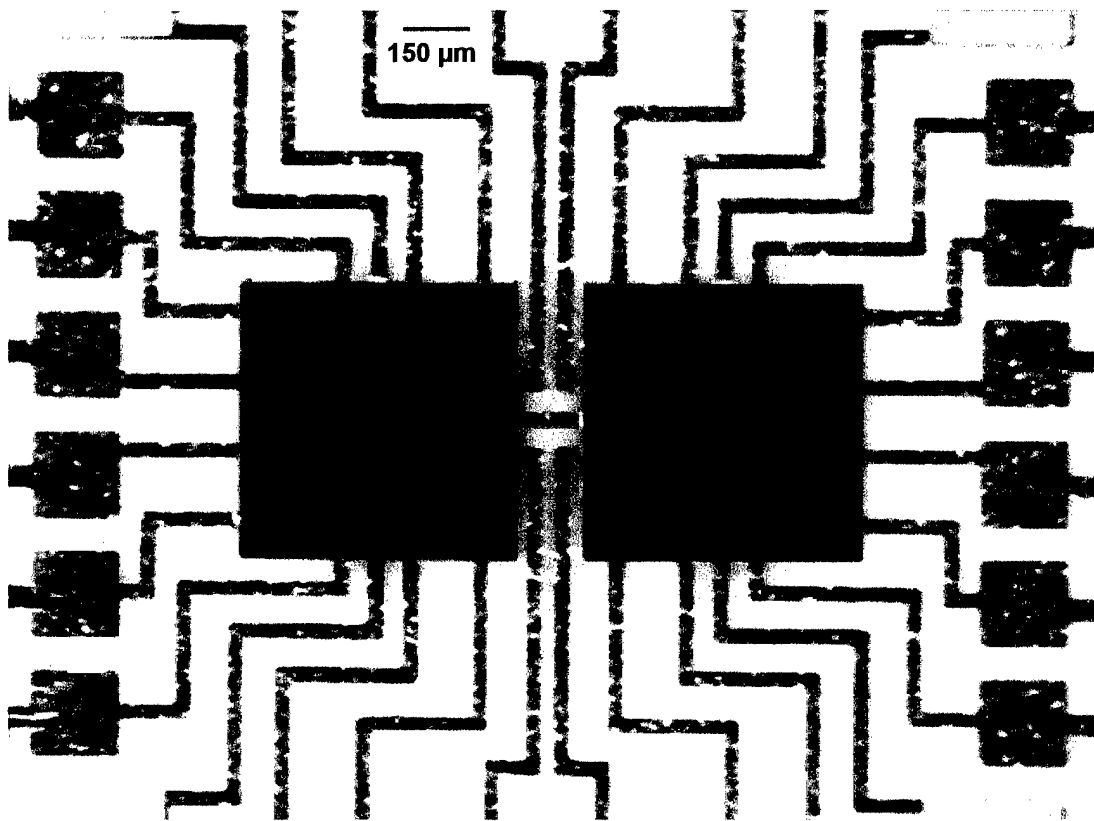
(a) Spent host module

(b) Released array on ceramic substrate

**Figure 6-18.** Photographs of host module and receiving substrate after release.

The spent silicon host module in Figure 6-18(a) shows four surfaces out of the array that were designed to float away with the host module so that the underlying address electrode and support structure of the devices could be visible on the ceramic substrate. Figure 6-18(b) shows one of the arrays fabricated using this technique in which it is obvious that the arrays were bonded with approximately 15  $\mu\text{m}$  of lateral alignment error. The effect of overetching is most visible in the rounded edges of the address electrodes that were initially drawn in rectangular shapes.

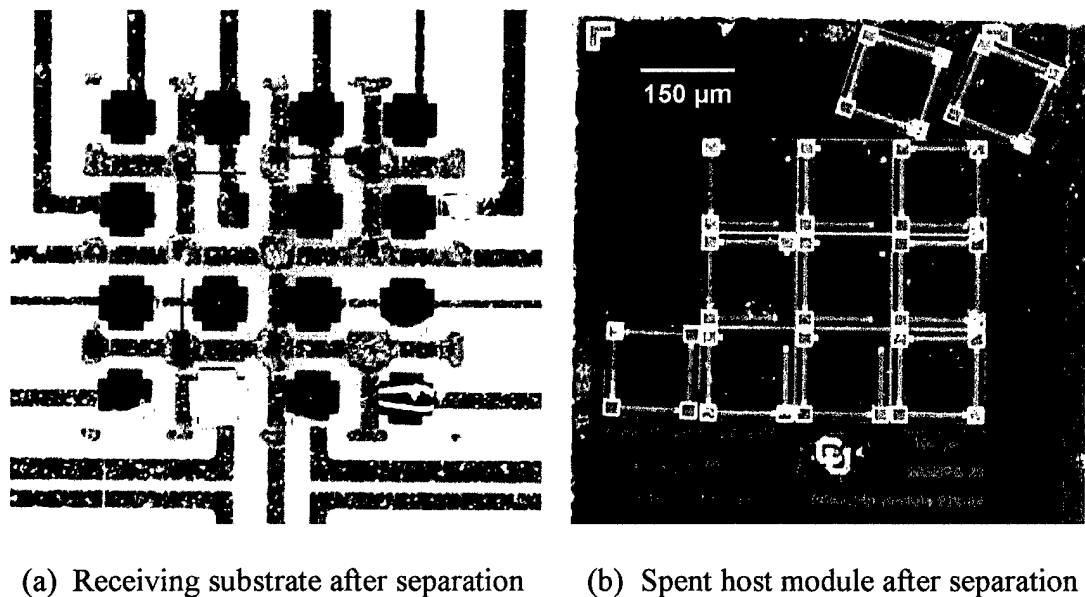
Numerous arrays of variable capacitors were fabricated in which each individual device within the array has its own bond pads with which to secure itself to the ceramic substrate. Provided sufficient ground lines exist within the array, the electrical performance of the variable capacitors is essentially the same. Each device has four bond pads to which the flexures are attached to secure the surface of the device. Figure 6-19 shows a typical released array of individually bonded devices.



**Figure 6-19.** Photograph of individually bonded devices on a ceramic substrate.

Although the preprocessing of the substrate is essentially the same as for the common bonding frame arrays, the bond pads within each device are considerably smaller which makes creating adequate gold and indium features slightly more difficult.

As a result of the smaller bond pads, the bonding yield of this design was slightly less than that of the arrays utilizing the common bonding frame surrounding each device. It was noted, however, that the success of each individual bond depended on the relative size of the pads and that more reliable bonds were repeatedly achieved with bond pads greater than  $40\text{ }\mu\text{m}$  square. For instance, the failed array of devices shown in Figure 6-20 serves to quantify a threshold in effective bond pad sizes below which the bonding yield drops considerably.



**Figure 6-20.** Photographs of failed arrays comprised of individually bonded devices.

The receiving substrate in Figure 6-20(a) shows that most of the  $70\text{--}80\text{ }\mu\text{m}$  square internal electrodes of the devices bonded properly. As shown in Figure 6-20(b), however, most of the  $25\text{ }\mu\text{m}$  square bond pads at the corners of each device failed to bond properly. These pads are visible on the host module in which many of the devices are still attached to the host substrate by oxide columns beneath the surface.

## **6.3 Yield Analysis**

Considering the two forms of arrays presented in this chapter, it is apparent that the common bonding frame produces the greatest yield such that more complete arrays were successfully transferred than with individually bonded devices. On average, slightly more than 70% of these arrays were bonded to ceramic substrates and demonstrated successful operation. Although many arrays showed adverse side effects from the bonding process, the devices typically behaved as desired.

For individually bonded devices, however, only 40% of the intended arrays bonded successfully. Any array in which even a single device failed to bond properly was considered a bonding failure and counted against the process yield. Many of these arrays failed by only one or two devices near the center of the array due to oxide columns that form during release. These columns are discussed in greater detail in the next chapter. Ultimately, each individual device actuated more like the desired behavior, but they were less likely to bond in complete arrays.

### **6.3.1 Primary Failure Mechanisms**

One of the primary concerns of this process is the indium contamination that is apparent after release of these arrays. During device actuation, these particles are electrostatically attracted to the address electrodes while resting on the grounded surface of the array. As a result, some devices and address lines were damaged when large particles came into contact with the grounded bonding frame and the electrodes beneath it. The devices simply burned up like fuses from the rush of current.

The other primary cause of concern for flip-chip bonding onto ceramic substrates is the effect of alignment error on the final arrays. Many of the poorly aligned arrays demonstrate adverse effects such as stress induced in the surface of the array and the flexures that support the surface of the devices. As a result, many of the devices did not deflect uniformly or did not rest in the desired position. Both of these characteristics alter the expected variable capacitance behavior of the entire array.

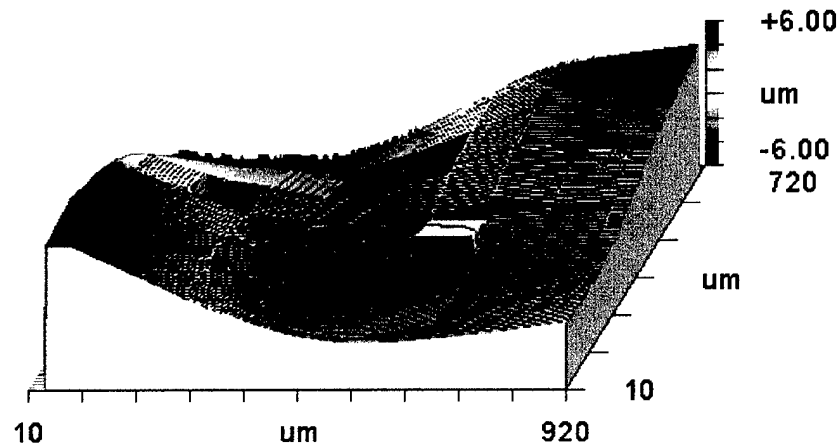
In some cases, the alignment error was so significant that the devices failed to actuate since the address electrodes were often shorted with the bond pads of the grounded bonding frame. This alignment error was sufficient to warrant the design of a new device and corresponding technique to enable flip-chip fabrication without the need for the flip-chip bonding machine. A latching off-chip hinge mechanism was designed to rotate host structures off the edge of a module so that they could be bonded onto ceramic substrates while keeping both modules visible under a microscope. It was later determined that this device was almost ideally suited to bonding integrated structures atop CMOS electronics. This feature is discussed in greater detail in the following chapters.

## **6.4 Device Performance**

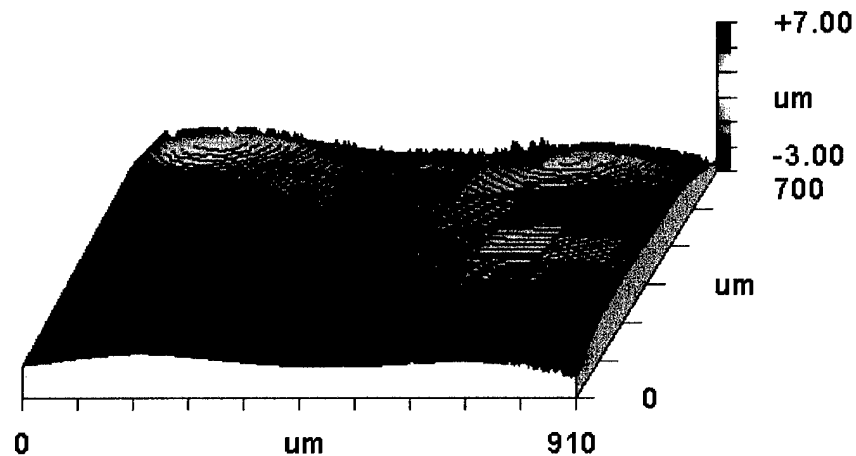
The piston variable capacitors fabricated on ceramic substrates were tested using the Zygo interferometric microscope. The primary concern was whether the arrays would deflect as designed and in a manner that was repeatable and predictable. This section describes the bonding results and the behavior of typical devices.

### 6.4.1 Bonding Characteristics

One disadvantage to this process is the stress that can be induced in the array due to slight alignment errors in rigidly attached bond pads. Figure 6-21(a) shows the result of this stress created by both the alignment error and internal stress of the pads.



(a) Deformation of array due to stress from alignment error between modules.



(b) Deformation of array due to thermal stress within bond pad layers.

**Figure 6-21.** Interferometric characterizations of early flip-chip capacitor arrays.

This array demonstrated nearly 8  $\mu\text{m}$  of peak-to-valley surface planarity variance across the 910  $\mu\text{m}$  array. Likewise, Figure 6-21(b) shows another effect of rigidly

attached bond pads on similar arrays. The bond pads are formed in gold and polysilicon which induces a stress due to thermal mismatch of the layers. Under this stress, the soft indium layer is susceptible to creep in which the bond pads slowly curl over time until the array becomes deformed. Figure 6-21(b) shows the best case of this problem in which 2-3  $\mu\text{m}$  of surface variance was characterized across the array. Several attempts to reflow the indium layer were made to reduce this variance, but all attempts made the problem worse by accelerating the creep process.

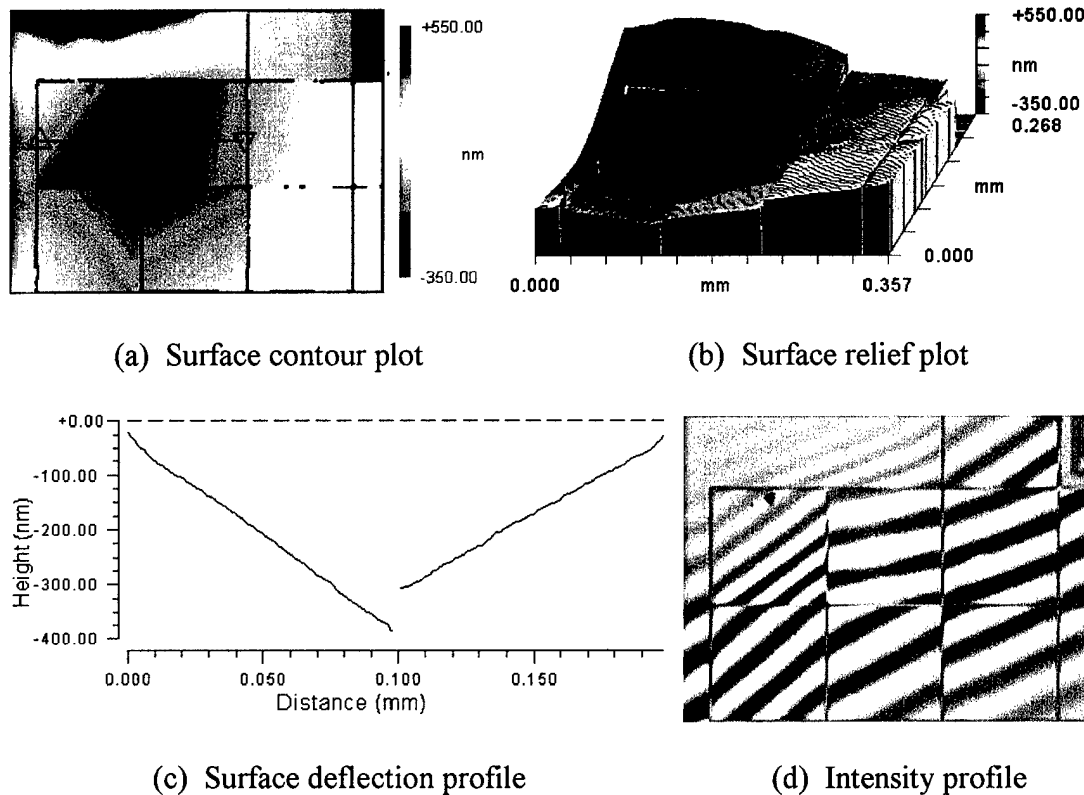
The flip-chip fabrication of polysilicon structures on ceramic substrates proved to be a success or failure depending on the particular application. In the case of variable capacitors, the arrays functioned completely as expected and the devices followed basic deflection models developed for piston style devices. To develop similar devices for use as micromirrors, however, produces numerous issues that simply could not be sufficiently controlled. It would appear that flip-chip assembly using indium layers on ceramic substrates is clearly not the technique of choice when the resulting arrays are expected to perform within optical tolerances. The planarity variances across the arrays and other issues inherent to the use of the indium layer are typically far more severe than can be tolerated by most optical specifications.

#### **6.4.2 Device Behavior**

Finally, the variable capacitor arrays were tested using an interferometric microscope which detects the position of each surface spanning the arrays. When repeated measurements are made during actuation, the deflection of a given device can be determined as a function of address potential which is the characteristic



behavior curve for the device. The arrays were first characterized in the resting position to find the relative flatness of the arrays. Figure 6-22 shows the result of this surface characterization for one of the worst-case local deformations.



**Figure 6-22.** Characterization of a common bonding frame variable capacitor array.

These plots indicate that the array has a base variance across the array which is most likely caused by the common back-plane that supports the individual devices. This support structure was intended to be used as a ground plane, but seems to be detrimental to the array as the four bonding pads have induced a stress in the structure that creates non-uniform resting positions for each flexure within the device and

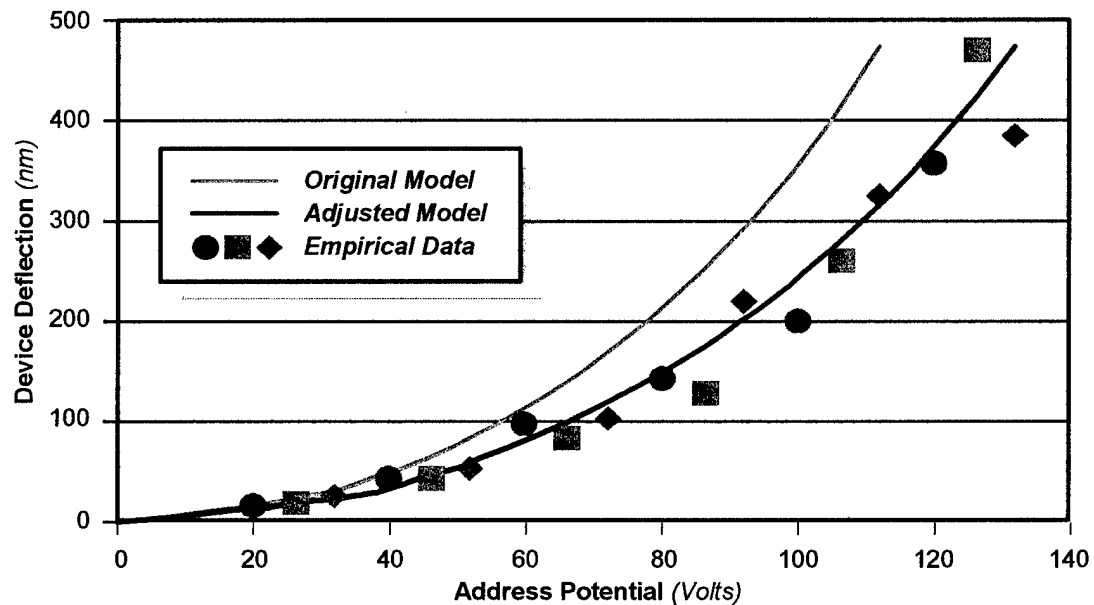
throughout the array. As a result, each mirror surface will be slightly tilted in a wave pattern across the array and will resemble a piece-wise linear surface.

The surface relief plot shown in Figure 6-22(b) reveals that this array demonstrates approximately 800 nm of surface variance across several devices. It should be noted that this plot is extremely exaggerated along the vertical scale to show the detail of the surface. Although the deflection appears to be excessive, each device is 100  $\mu\text{m}$  square resulting in roughly  $0.20^\circ$  of maximum tilt. This level of planarity is still favorably comparable to ordinary surface-micromachined devices. The bond pad shown in the upper left corner rises above the surface of the remaining array in an irregular pattern indicating the presence of induced stress in the structure.

Additionally, Figure 6-22(c) illustrates that each surface is actually quite flat, demonstrating only 2-3 nm of RMS surface roughness across the device. This cross section profile is given by the line drawn in Figure 6-22(a) across two devices. This level of flatness is unprecedented in surface-micromachined devices with the support structures located beneath the surface. Normally, extreme topographical effects scar the surface. The only means of removing this error is to modify the process at great expense to add a planarization step which can still produce as much as 150 nm of surface variance across such devices [2]. In short, no surface-micromachined devices have demonstrated this degree of optical flatness without using advanced and often expensive fabrication techniques.

To determine the characteristic behavior curve of typical piston devices, a similar surface characterization was made for the same set of variable capacitors in each array at various address potentials. The surface deflection profile such as the

plot shown in Figure 6-22(c) provides very accurate deflection data for specific points along the mirror surface. Collecting deflection versus address potential data provides the characteristic behavior curve shown in Figure 6-23 for three similar devices. Both original and adjusted model curves are shown along with empirical data.



**Figure 6-23.** Characteristic behavior of three typical piston variable capacitors.

The original model trace is the predicted behavior of the devices given the design dimensions and the ideal operating characteristics of the array such as near static drive frequency and negligible stress in the support structure. The adjusted model curve represents the changes in these characteristics based on observed conditions such as the reduced area of the address electrodes and the induced stress in the support structure. This induced stress creates added resistance in the flexures during actuation. They become less compliant and therefore the device spring constant and required address potential increase in order to achieve a desired deflection.

The data traces represent the center of three identical devices located within a single array. Although each trace is not perfectly shaped as the model curve, they all obey the general relation of deflection versus address potential sufficiently to validate successful fabrication of the devices. The slightly varied curves can be attributed to the induced stress in the support structure that creates a non-uniform deflection distribution across the array. Only the center of the device is characterized and the plot in Figure 6-23 does not represent the slight tilting along two axes that may occur as the device deflects. This plot does represent a general behavior curve that is very consistent between devices across the array.

## **6.5 Conclusions**

The variable capacitor arrays presented in this chapter were bonded to ceramic substrates patterned with gold wires, address electrodes, and bond pads using a thin layer of indium for adhesion. Although some arrays demonstrated lateral slipping or alignment errors during bonding, this process was capable of successfully bonding the silicon host module to the ceramic substrate. After release, the silicon host substrate floated away leaving the released devices attached to the ceramic substrate.

Although some adverse effects were observed in these first generation arrays, it should be noted that these effects were still within controllable limits and were typically the result of pushing the design rules of the flip-chip process in order to obtain highly optimized performance of the devices. Regardless, these devices behaved according to an advanced model that describes the typical deflection

behavior of such devices as a function of address potential and demonstrated an unprecedented non-planarized optical flatness of only 2-3 nm of RMS surface roughness across as much as 150  $\mu\text{m}$  square surfaces. Some variations in the deflection data were observed and attributed to induced stress in the support structure of the devices due to the alignment errors. Given next generation arrays, these adverse effects could be virtually eliminated by improved design.

This research clearly demonstrates that surface-micromachined structures can be flip-chip bonded onto other receiving substrates which offer better properties for any given application. This flip-chip process leverages optimized fabrication services rather than attempting to duplicate the service using specific materials. As a result, advanced MEMS structures can now be fabricated on virtually any non-silicon work surface using a low-cost, simple and reliable flip-chip assembly technique.

## **CHAPTER 7**

### **FLIP-CHIP ASSEMBLY ONTO SUBMOUNT MODULES**

This chapter describes the process by which surface-micromachined structures from one flip-chip module are transferred to those of another. The advanced micromirror arrays presented in this chapter were created using a novel, inexpensive, simple, reliable, and repeatable post-process flip-chip assembly technique. The arrays were assembled by flip-chip bonding the upper structural layers of a micromirror array host module to the lower structural layers of a receiving submount module using a custom built flip-chip bonding machine. Each chip was commercially prefabricated in the MUMPS process and then flip-chip bonded to form the working arrays such that many of the typical adverse effects of surface-micromachining were removed. Very little preprocessing of the commercially prefabricated chips was required to perform the flip-chip transfer technique since the devices are formed by directly fusing the gold layers of the MUMPS process.

Several arrays of piston, cantilever, and torsion style micromirror devices were flip-chip assembled using this technique. For each of the arrays, the micromirror host module and the receiving submount module are both prefabricated as part of the same MUMPS run where each of the delivered 1 cm square chips can

be sub-diced into as many as 100 smaller modules. These arrays demonstrate highly desirable features such as 98% active surface area, five structural layers, planarized reflective surfaces boasting less than 2 nm of RMS surface roughness, address potentials compatible with CMOS control electronics, less than 80 nm of peak planarity variance across 1 mm arrays and built-in masking capabilities for deposition of reflective materials. A variety of bonding features and design techniques were developed to correct for slight misalignment errors during bonding and typically result in less than 2  $\mu\text{m}$  of lateral alignment error.

This work demonstrates that the demanding requirements of most micromirror applications can be met using a fast, simple, and low-cost technique that produces devices comparable or even superior to those fabricated using far more costly techniques. Ultimately, the standard thermo-compression flip-chip assembly process remains a viable technique to develop highly complex prototypes of advanced micromirror arrays or other advanced MEMS components.

## **7.1 Introduction**

As described in Chapter 2, one of the most enabling features of any MEMS fabrication service is the number of structural layers available to the designer of surface-micromachined components [2]. The complexity and capabilities of such devices increases significantly with the number of structural layers since more intricate mechanisms can be created and there are more choices in the thickness and height of any desired structure. Commercial foundries, however, limit designers to

very few choices of materials or number of structural layers. As a result, it may not be possible to create many specialized devices required for more demanding applications without custom fabrication methods which are usually very expensive. As an alternative, highly complex structures can be made by flip-chip bonding surface-micromachined features onto a variety of other substrates or even other chips fabricated in the same process. The original silicon host substrate is then removed during the release etch to produce highly advanced MEMS that are better suited to RF, microwave, or optical applications where specific material properties or additional structural layers are required [20].

The flip-chip assembly technique allows designers to use the layers from at least two separate MUMPs modules. As a result, there are at least five structural layers available to create advanced devices rather than the three layers on a single chip. The upper portion of the flip-chip device is patterned in the releasable layers of the host module while the lower portion of the device is fabricated on the receiving module and fully anchored to the substrate [20]. To facilitate the disposal of the host substrate during the release etch, the features on the host module are not anchored to the substrate, but are only supported by the sacrificial oxide layers [10]. Therefore, the lowest layer of the process is not available for design on the host module.

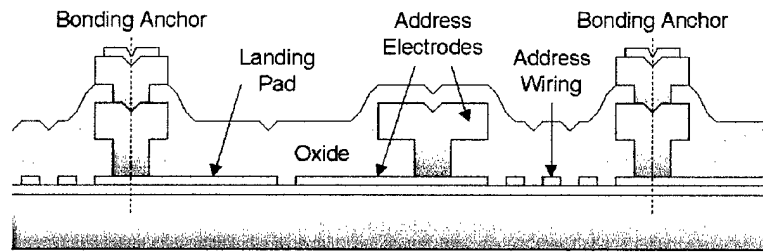
The flip-chip modules used to create the micromirror arrays were prefabricated in the MUMPs process which offers three structural layers of polysilicon and a final layer of gold. Unfortunately, this process does not provide planarization so features patterned in the upper layers will conform to features patterned in lower layers. Normally, these topographical effects would render



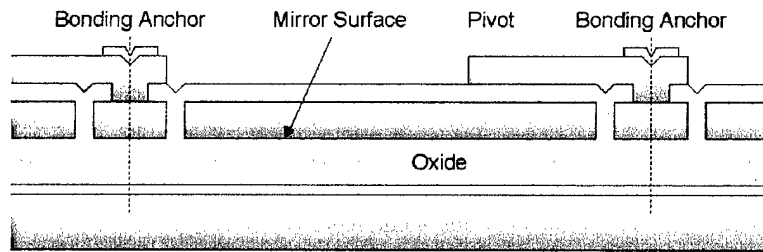
micromirror surfaces virtually worthless if the flexures and electrodes of the device were patterned beneath it [21]. With flip-chip assembly, however, the chips can still be fabricated in the lower cost MUMPs process, but with some features of more expensive services. The final devices are highly planarized since the mirror surface was fabricated as the underside of the lowest layer on the host module. Likewise, mirror elements can reliably be segmented in any pattern desired. Without features patterned beneath it, this layer consistently shows less than 2 nm of RMS roughness.

The various flip-chip micromirror arrays presented in this chapter were fabricated in three phases. First, the receiving module is designed with bond pads and support features that are intended to anchor the layers from another surface-micromachined host module. Figure 7-1(a) shows a typical receiving submount module which contains the address wiring, address electrodes, probe pads and lower flip-chip bonding structures.

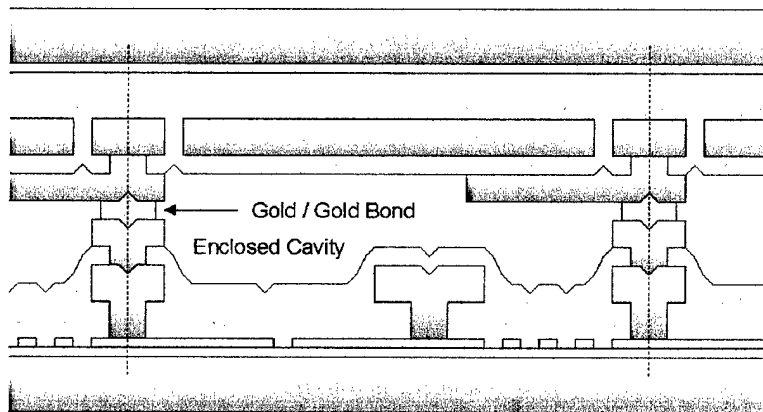
Then, the host module is designed with opposing bond pads and support features attached to the surface of each micromirror device. Both the host module and the receiving module can be fabricated as part of the same prefabrication process. Figure 7-1(b) shows a typical cantilever micromirror host module containing the mirror surface formed in the lower structural layer and the flexures, pivots, and upper bonding structures formed in the upper structural layer. These features are supported only by the first oxide layer and are not directly anchored to the substrate such that they will separate from the substrate when the oxide between them is removed [20].



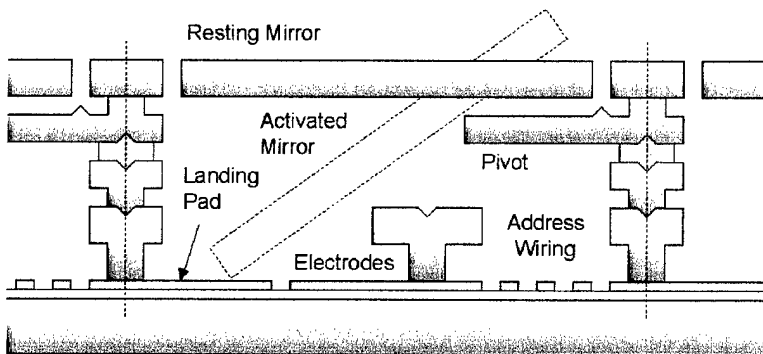
(a) Illustration of a cantilever micromirror receiving cell.



(b) Illustration of a cantilever micromirror host cell.



(c) Illustration of alignment and bonding of flip-chip modules.



(d) Illustration of release and activation of resulting cantilever device.

**Figure 7-1.** Illustration of the typical submount flip-chip assembly process.

Once delivered from the foundry and diced into separate chips, the modules are bonded using a custom-built flip-chip bonding machine. The host module is inverted and bonded to the receiving module using the gold layer of the MUMPS process used to form bonding features on both modules. Figure 7-1(c) illustrates this bonding step and shows the gold/gold bond between the flip-chip modules and the enclosed cavity that is sometimes created between them.

Finally, the bonded modules are released in a standard etch to remove the oxide between them. Since the upper layers of the micromirror devices are supported only by oxide and not rigidly anchored to the original silicon host substrate, the substrate is discarded and simply floats away during the release etch [10]. The resulting devices have five structural layers of polysilicon bonded with a thin layer of gold. Figure 7-1(d) shows a typical cantilever micromirror device in the resting and actuated positions. The mirror surface rests in a stable actuated position against a landing pad and pivot which can be designed to produce a precise tilt angle. As described throughout this chapter, a torsion device is created simply by designing two cantilever structures along opposite sides of the axis of rotation.

As illustrated in Figure 7-1(d), the mirror surface of the device rests much closer to the address electrode when deflected to the stable position. Since the electrostatic force supplied by these address electrodes increases as the gap between the plates decreases, the address potential required to hold a deflected mirror surface is often significantly less than the potential required to initially deflect it. The second elevated address electrode shown in Figure 7-1(d) is designed to reduce the original gap and therefore the address potential required to actuate the device.

### 7.1.1 Background

The original motivation for the development of the general flip-chip assembly technique was to create highly miniaturized variable capacitors for RF applications. Although a wide variety of surface-micromachined devices were well suited to RF circuits, the silicon substrates upon which they were typically fabricated induce severe charging effects that render the devices useless. The most immediate and cost-effective solution was to assemble surface-micromachined devices on a ceramic substrate patterned with gold wires [10]. This approach has demonstrated several types of variable capacitors on ceramic substrates and is uniquely enabled by the flip-chip assembly technique [20].

This project has since expanded to include the fabrication of highly advanced structures by flip-chip bonding MEMS components to other MEMS substrates. Many of the lessons learned from the original ceramic substrate research were applied to this form of flip-chip bonding such that a large number of working devices was almost immediately realized. For instance, the rigid bond pads in many of the original ceramic substrate arrays produce a much higher rate of successful bonding.

The purpose of this research is to develop a simple, reliable, repeatable, and inexpensive post-process assembly technique that would make use of existing commercial fabrication services, yet provide the greater flexibility that designers demand for advanced applications. Numerous foundries have already spent significant time and money to fully optimize MEMS fabrication processes for increased yield, turn-around time, and reduced cost. Therefore, rather than develop a new fabrication service, a novel post-process flip-chip assembly technique could be

used that would leverage the existing fabrication industry and would be far more efficient and realizable. Reducing such a flip-chip assembly technique to practice would allow designers to transfer application-specific devices to a variety of desired work surfaces or assemble highly complex devices and integrated microsystems. Ultimately, the development of such a novel flip-chip assembly process offers a means to create advanced systems which are currently not achievable.

By applying the lessons learned from the original flip-chip bonding of host structures on ceramic substrates, the first attempts to produce submount micromirror arrays were a surprising success and spawned several generations of more advanced arrays. Many of the design concepts and bonding techniques developed as part of the early research are discussed in this chapter in relation to improvements made for the purpose of producing submount flip-chip structures.

### **7.1.2 Applications**

Since the purpose of this research is to develop a novel technique by which advanced MEMS can be created, the applications that are enabled by this technology are too numerous to identify and are effectively limitless. As described in Chapter 2, the complexity and therefore the capabilities of any MEMS component increase with the number of available structural layers available to the designer. As a result, any application involving complex latching, switching, sensing, or actuating needs can be enhanced by flip-chip assembly. Although this chapter deals solely with micromirror arrays, optical applications are only a small portion of the potential disciplines that would benefit from submount flip-chip bonding.

### 7.1.3 Advantages

One of the greatest benefits of this form of flip-chip fabrication is the ability to use existing foundry services for commercial prefabrication of flip-chip modules. The gold layer available in the MUMPs process makes flip-chip assembly a simple, fast and inexpensive means to create highly advanced micromirror arrays. Since the layers from the two modules are directly fused during bonding, there is very little preprocessing required before assembly. Additionally, each of the 1 cm square chips delivered from the foundry can be divided into as many as 100 standardized multiples of 1 mm square modules to facilitate easy dicing after fabrication. In this manner, numerous researchers can share portions of the entire chip and the cost to produce it so that the cost of flip-chip assembly of prototype devices is considerably reduced.

As previously described in Chapter 3, another primary benefit of flip-chip assembly is the inherent planarization of the flip-chip structures. The upper layers of a flip-chip assembled structure are fabricated on a separate host substrate such that no topographical effects are created in the surface by lower layers. As a result, problems typically associated with mechanical linkages, variable capacitors, and virtually all optical components can easily be eliminated by design of flip-chip devices. This effective planarization of flip-chip structures is universal to the process such that all flip-chip devices demonstrate less than 2 nm of RMS roughness. A detailed study of planarized structures is presented in Chapter 9 in which a statistical analysis of numerous micromirror arrays found this to be a common feature of the process.

As mentioned in Chapter 2, the complexity of a MEMS component increases sharply with the number of structural layers available to the designer. More intricate

structures are capable of performing more tasks or optimizing the performance of others. Using the flip-chip assembly process, the features from one module can be transferred to another module such that the total number of structural layers is increased beyond the foundry limit of the prefabrication process. For instance, the flip-chip modules presented in this chapter were prefabricated in the MUMPS process which offers only three structural layers. However, the resulting flip-chip devices boast five structural layers and therefore much greater versatility and performance over standard micromirror devices.

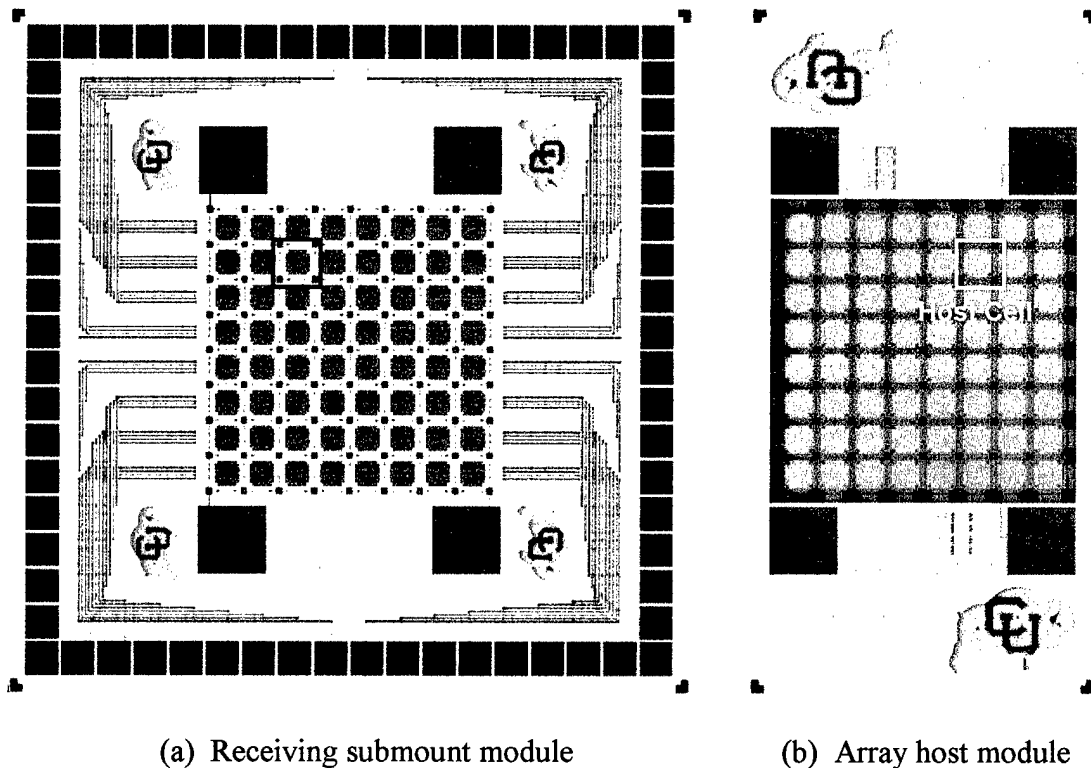
#### **7.1.4 Disadvantages**

Probably the most significant disadvantage to this form of flip-chip assembly is the need for highly specialized equipment. The flip-chip assembly technique requires a custom-built, computer-controlled machine to facilitate and regulate the bonding process. Although somewhat similar machines can be purchased for some flip-chip purposes, the equipment used to perform this research was not commercially available and can cost a considerable amount of time and money to build.

The flip-chip bonding machine required for this assembly technique is also the source of another problem common to this process. Without repeated calibrations, the machine can demonstrate significant alignment errors between host and receiving modules that sometimes produce disabled or even inoperable devices. Although this error can be minimized by both design of modules and bonding technique, the ability to bond two features within a required alignment tolerance will always be an issue.

## 7.2 Implementation

Although the design and fabrication of the host module and the corresponding receiving module are critical to successful flip-chip assembly, the basic concept of their design is really quite simple. A typical pair of flip-chip modules is shown in Figure 7-2 illustrating an early design of submount modules used in this research.



**Figure 7-2.** Layout diagrams of piston micromirror array flip-chip modules.

These modules produce a rectangular  $8 \times 8$  array of individually addressed piston micromirror devices that are connected by a common bonding frame surrounding each device. As described in previous chapters, this frame can reduce the complexity of each individual device and increase the probability of a successful bond.



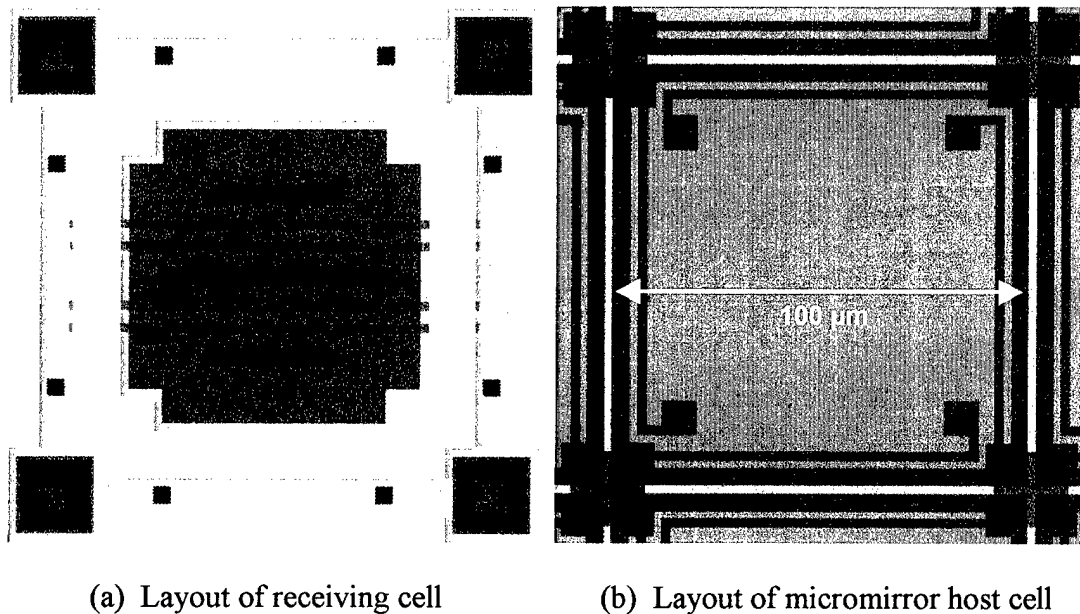
The receiving submount module shown in Figure 7-2(a) is 2 mm square and contains the address wiring, electrodes, probe pads, and support structure for the final assembled array. The address electrodes were elevated to reduce the address potential required to actuate the devices and to allow the wiring to devices in the center of the array to run beneath them. The micromirror array host chip shown in Figure 7-2(b) is 1×2 mm and contains the top of the micromirror devices and upper support structure formed in the upper two layers of the process. These layers are not anchored to the substrate so that they separate upon release. The host module was designed to be smaller than the receiving module to facilitate handling once bonded. All structures on the modules are drawn well within a 50  $\mu\text{m}$  margin in order to create at least a 100  $\mu\text{m}$  dicing channel between each module.

The two flip chip modules are drawn as mirror images of each other such that the outlined micromirror host cell in Figure 7-2(b) is bonded atop the corresponding receiver cell in Figure 7-2(a) once the host module is inverted and bonded. Both modules typically share a common bonding assembly that anchors the mirror surfaces by compliant flexures to a support frame surrounding each device within the array. The four large bond pads are connected to the arrays by flexures to remove stress due to slight misalignments between pads. Although the small gold features drawn within each device are sufficient to bond the flip-chip modules, the large bond pads contain topographically opposed dimples that help to guide the chips into position during bonding to remove slight alignment errors.

The gold layer of the MUMPS process simplifies this type of flip-chip assembly by allowing direct gold-to-gold bonding of the flip-chip modules. Although

a variety of adhesion materials can be used, this technique requires very little preprocessing of the bonding modules to facilitate the assembly technique.

The individual address cell shown in Figure 7-3(a) illustrates the elevated address electrode below which internal devices can be wired. The mirror host cell in Figure 7-3(b) shows the flexures and opposing bond pads that complete the device.



**Figure 7-3.** Layout of typical rectangular piston flip-chip micromirror elements.

The adverse topographical effects normally observed in surface micromachining processes are not a factor in flip-chip assembled devices since the upper and lower layers are prefabricated on separate chips. All that is necessary is that the gold bond pads or other gold bonding features are the tallest structures on both chips. In designing a variety of custom devices, it is critical to note the combined clearance of the opposing gold bonding features to ensure that they are free to make contact before other structures across the modules.

### 7.2.1 Bonding Techniques

Unfortunately, the flip-chip bonding process can be somewhat sensitive to the lateral alignment of the host module features to those on the receiving module [21]. Slight misalignments induced by the flip-chip bonding machine can create large variations in device performance while some devices can be rendered completely useless if the alignment error exceeds the tolerance for that device.

The means by which a host chip will be aligned to the receiving chip must be carefully considered during the design of the modules. The resolution of the bonding machine camera system is not sufficient to view flexures or other smaller markings that determine whether each module is correctly oriented to the other. Some arrays were designed with a unique axis of symmetry so that improper orientation was not a concern. For instance, the polar distribution of one piston array made it easy to detect if the chips were rotated  $90^\circ$  from the proper orientation. Due to the array symmetry, it does not matter in which direction the chips are turned to correct the error. The cantilever arrays, however, are far more sensitive to orientation. Such devices can only deflect in one direction relative to the receiving module, so great care must be taken to ensure proper orientation during bonding. Therefore, additional alignment marks must be used which are visible through the camera system. Complementary portions of easily distinguishable shapes are asymmetrically placed on both modules so they form a recognizable pattern only when the modules are properly oriented [22].

Although the bonding machine camera system can be repeatedly calibrated to remove the majority of the alignment error, many flip-chip micromirror arrays have been designed with bond pad features that help reduce alignment error or increase the

alignment tolerance of individual devices. Table 7-1 summarizes the formation of the micromirror devices within two specific types of array implementations and lists the primary alignment feature employed for each array.

**Table 7-1.** Summary of flip-chip module bonding technique and alignment feature.

Micromirror Array	Host Module	Receiving Module	Bonding Technique	Alignment Feature
<b><i>Polar Piston</i></b>	Mirror Surface Only	Complete Actuator	Individual Device	Large Bond Pad
<b><i>Cantilever, Rectangular Piston</i></b>	Upper Actuator Plate	Lower Actuator Plate(s)	Common Frame	Dimpled Bond Pads

The first alignment feature is a single large bond pad placed within each device on both the host and receiving modules. For polar piston arrays, the pads were placed on each mirror surface and corresponding actuator. These large gold pads are roughly 80  $\mu\text{m}$  in diameter and designed to be much larger than the expected alignment error of the bonding machine which virtually assures that the pads will sufficiently bond to form the working device. The complete actuator on the receiving module is unaffected by position error in the placement of the mirror surface.

The second alignment feature is the combination of topographically opposed dimpled bond pads that fit together only when properly aligned [22]. These pads are usually placed at each corner of the flip-chip modules or along the edges of arrays that are supported by a common frame. The opposing dimples are designed to correct for slight alignment errors by inducing an uneven stress along the surface of the dimples which forces the pads into alignment during the bonding process [22].

### 7.2.2 Design of Piston Devices

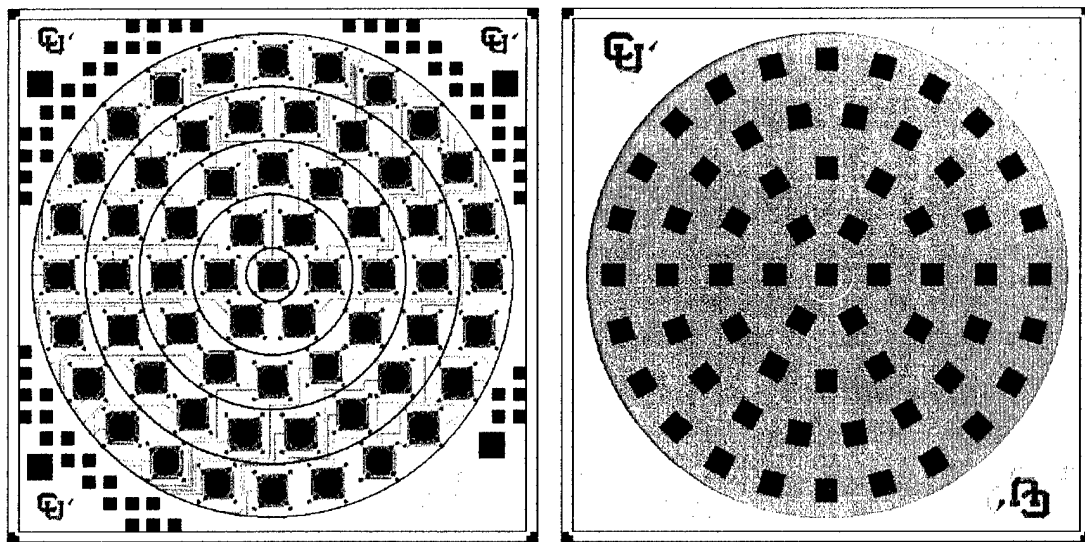
The initial piston array designed for submount bonding is the rectangular array shown in Figure 7-2 in which a common bonding frame is used to anchor the devices to the receiving module. As previously described, each device was created by bonding the mirror surface, flexures, and host support structure from the host module to the receiving support structure on the receiving module containing the address electrode, wiring, and probe pads. This array and several similar designs performed so well that numerous iterations and more advanced arrays were designed and fabricated. This section describes the design of the first polar piston micromirror arrays originally created after the success of these early rectangular arrays.

As noted in Table 1, the polar piston arrays were designed with complete actuators on the receiving module such that only the reflective surface of each device is transferred during the bonding process. As a result, all actuators within the array and between different arrays tend to function identically regardless of the placement of the mirror surface. Using this method, however, induces two other concerns.

First, although the individual alignment tolerance has increased, the planarity tolerance between the host and receiving modules has decreased. The bonding machine must be carefully calibrated to ensure planarity between the two modules so that each individual pair of bond pads makes contact with sufficient force to bond.

The second concern is curvature induced in the mirror surface. With the large gold bond pad used to increase the alignment tolerance, the residual stress from the thermal mismatch between the gold and polysilicon layers forming the bond pad will create a slight distortion in the surface. This effect can be virtually eliminated by

using a minimally connected mirror supported only by a small post in the center of the bond pad. Such a device, however, is more susceptible to damage during bonding and even more so during release. As a first generation demonstration, a slight curvature in each mirror surface was preferable to incomplete or damaged arrays. Figure 7-4 shows a pair of typical polar piston micromirror flip-chip modules.



(a) Actuator receiving module layout      (b) Micromirror host module layout

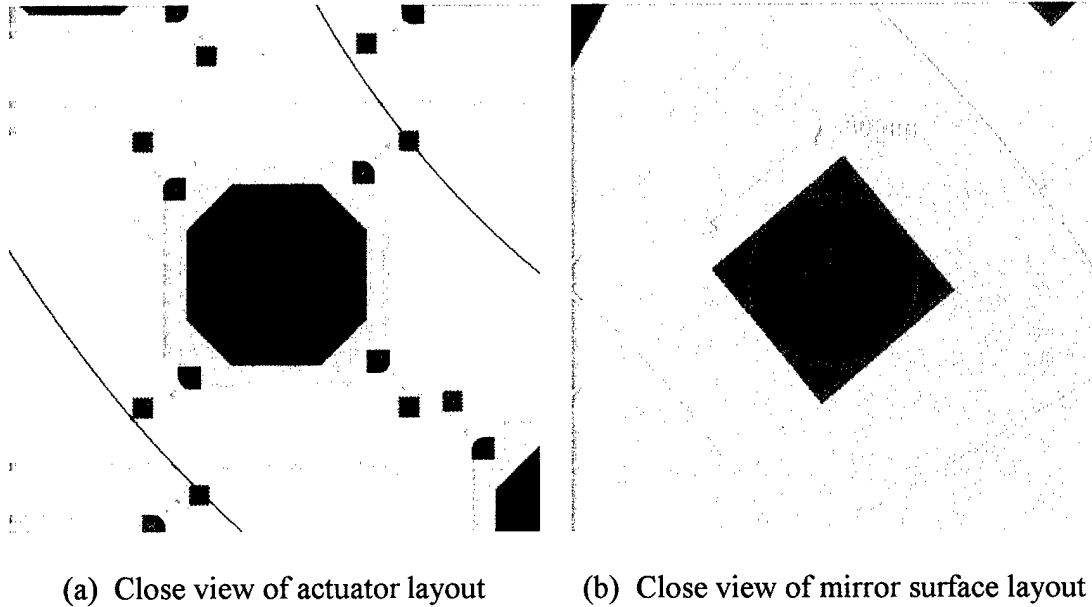
**Figure 7-4.** Layout diagrams of polar piston micromirror array flip-chip modules.

The primary benefit of individual device bonding is that complete actuators are identically formed on the same module so that they demonstrate consistent behavior. Likewise, each module is fabricated on the same MUMPs chip which suggests consistent behavior between arrays. Devices that are formed by joining plates from different modules, on the other hand, are far more susceptible to performance variations due to bonding since the position of the upper electrode and flexures has a significant electrostatic and mechanical influence on the performance of the device.

To increase this benefit and also the simplicity of design, a standardized actuator is placed at the center of the desired mirror surface element which can then be segmented independently. As shown in Figure 7-4(a), the fully formed actuators are distributed along a polar coordinate system where the center of the actuator bond pad is located precisely where the center of the mirror elements in Figure 7-4(b) are to be placed. The design of the actuators and the segmentation of the mirror surface of the array are completely independent of each other which enables a variety of shapes and designs of arrays that can be custom fit to specific optical aberrations [23].

The actuators in the array are distributed along a polar system in four distinct 200  $\mu\text{m}$  wide bands of 6, 12, 18, and 24 devices surrounding a single central device resulting in 61 individually addressed elements. To increase performance uniformity, a grounded polysilicon plane surrounds all actuators, as shown in Figure 7-4(a), so that each is electrostatically isolated from the electrodes of other actuators regardless of proximity within the array. Additionally, although distributed along a polar system, all actuators remain oriented along a rectangular system used by the foundry to generate the photomasks used in fabrication. These masks are generated by snapping all curves and other complex shapes to a rectangular grid in order to pixelize each feature in the layout. As a result, identical actuators drawn at various rotated angles to the grid produce flexures of varying widths and therefore varying spring constants. The result is a much wider range of behavior between actuators and even some actuators that tilt while deflecting. Although smaller grid sizes of high-quality services produce little deformation, it is already known that the MUMPS grid size is more than sufficient to produce malformed or even nonfunctional flexures [12].

The actuators within this array were designed to fully deflect through 650 nm at approximately 5 volts in order to be compatible with CMOS control electronics. Figure 7-5 shows a closer view of the layout of the opposing actuator and mirror surface cells that are bonded together to form the working device.



**Figure 7-5.** Layout of typical polar piston micromirror array flip-chip elements.

The edges of all features within the actuator shown in Figure 7-5(a) were rounded to remove stress concentrations and to produce flexures that behave more like ideal springs rather than flexures with sharp corners which require torsion analysis [14]. As described in Chapter 5, flexures with such features behave like stiffer springs than flexures of the same total length that are drawn as a straight beam. The octagonal address plate in the center of the actuator was inserted to ensure that the gold bond pad above the actuator was the tallest feature on the module. These actuators have deflection stop posts to prevent shorting of the devices should the surfaces collapse.



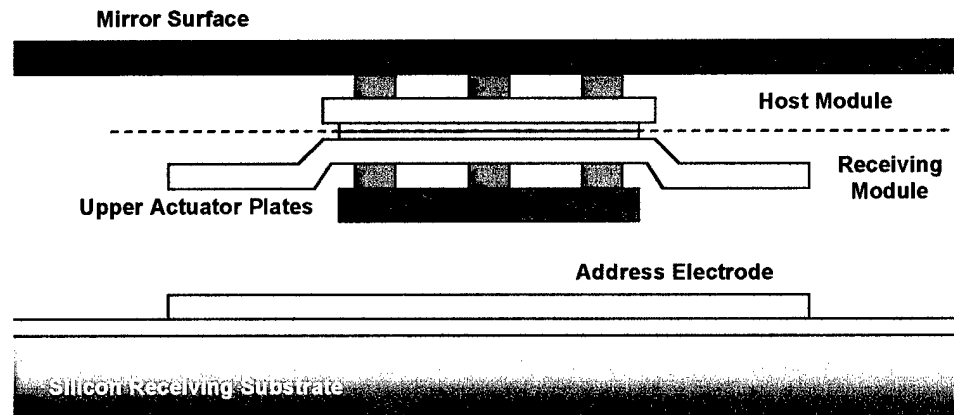
The ground plane surrounding each device is also visible in Figure 7-5(a) in which the flexures are simply cut from a uniform layer of the upper polysilicon. Without this ground plane, stray electric field lines would interfere with adjacent devices within the array since each surface is much larger than its actuator. Small holes are cut in the stops located at the ends of the flexures so that small columns in the upper polysilicon layer do not interfere with the operation of the device. Such features are typically formed when upper layers fill in anchors beneath them.

As shown in Figure 7-5(b), the size and shape of the mirror surface are both independent of the actuator beneath it. The surface bond pad shown in Figure 7-5(b) is roughly 80  $\mu\text{m}$  in diameter and is anchored by four support posts placed at opposite corners surrounding the pad. Although this design was expected to create some curvature in the final surface of the bonded device, the magnitude of the curvature and its effect on the bond between the two cells was initially unknown.

To reduce diffraction effects that may be observed when using this array, the entire array surface was intentionally segmented so that no mirror edges within a single polar band line up with the edges of adjacent bands. In this manner, only two corners of adjacent devices will meet along the continuous edge of a third device rather than all four corners meeting as is typical with standard rectangular arrays. Figure 7-5(b) illustrates this optimized segmentation showing only 2  $\mu\text{m}$  gaps between mirror surfaces. Since no etch holes were placed in the surface of these devices, each 1.8 mm diameter planarized array boasts 98.3% active surface area.

When the two opposing flip-chip modules are finally bonded, the resulting piston device should behave just as the independent actuator since the mirror surface

does not interfere with either the electrostatic force or the restoring spring force of the device. Therefore, the bonded device shown in Figure 7-6 can be sized and shaped to virtually any specification based solely on the needs of the application.



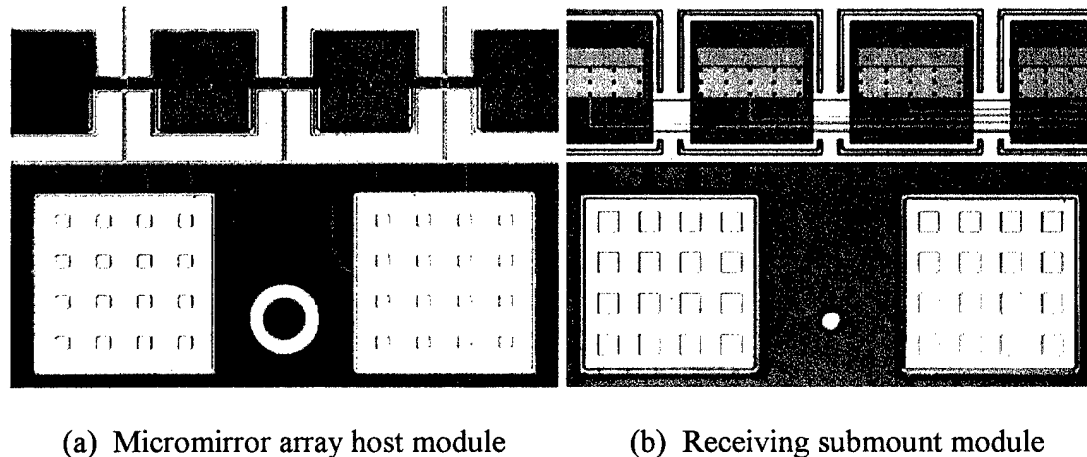
**Figure 7-6.** Side view illustration of bonded polar piston micromirror element.

This figure only illustrates the final nomenclature of the bonded device and does not show the ground plane or flexures surrounding the upper actuator plates.

### **7.2.3 Design of Cantilever Devices**

Similar to the early piston style devices, numerous cantilever arrays were assembled using the same design concepts and assembly procedures. Unlike the piston devices, however, these arrays demonstrated adverse characteristics that had to be addressed in next-generation designs. For instance, many of the early cantilever arrays were designed without a grounded landing pad for the mirror surface in the fully deflected position. As a result, charging effects on the surface of the substrate created stiction problems that resulted in reduced switching capabilities.

Although many of the original cantilever arrays used the same bonding frame surrounding each device, the original implementation of that frame caused problems during fabrication. For instance, the bonding frame surrounding the host cells and the receiving cells in Figure 7-7 were drawn with a continuous layer of gold.



**Figure 7-7.** Photographs of typical cantilever micromirror array flip-chip modules.

Once these modules are bonded, the continuous layer of gold forms a tight bond around each cell and produces an enclosed cavity within each device. As indicated in Figure 7-1(c), this cavity can only be released once the HF flows beneath the frame from the adjacent device. As a result, the central devices within the array did not begin to etch until the outer devices had already been released. This increased the total time of the release etch and could potentially damage some of the devices. To reduce the effect of this design, all subsequent cantilever arrays were designed with segmented gold pads to allow the HF to immediately reach all devices during release.

Also shown in Figure 7-7 are the flexures that connect the large bond pads to the bonding frame holding the devices. These flexures were originally drawn with

sharp corners at the interface with the frame and bond pads which often fractured during bonding. Although still encased in oxide, the stress concentrated at these interface points was often sufficient to break the flexures. Later designs of flexures were drawn with rounded features at these interfaces which eliminated the problem.

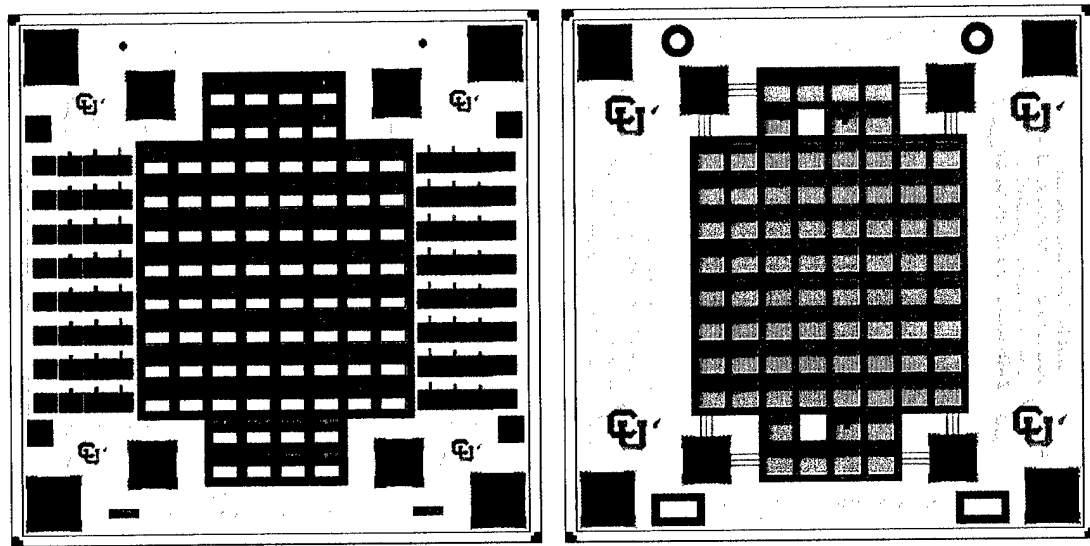
The receiving cells shown in Figure 7-7(b) also illustrate two design features that had to be corrected in later arrays. First, the mirror surface was originally designed to land on the nitride layer on the receiving substrate when the device was fully actuated. As previously described, this leads to charging effects that hold the mirror surface in the deflected position long after the address potential is removed. As illustrated in Figure 7-1(d), a grounded landing pad was later added to each device to remove this effect and maximize the device switching capability.

Also shown in Figure 7-7(b) are the address wires running through each device and the large address electrode exposed to the mirror surface. The electrostatic force supplied by these address wires and the inner portion of the address electrodes acting on the opposing side of the mirror is sufficient to produce a wide variety of device behavior. In order to create more uniform actuation within the array, a grounded shield was later designed to rest over these wires and adjacent to the address electrode to minimize the stray electrostatic forces they create.

Employing these lessons from early arrays, the next generation cantilever arrays were designed with specific requirements set by the sponsor of this research. Although by far the most numerous and widely varied in design, most arrays have a few specific similarities. As noted in Table 1, the devices within each array are supported by a common bonding frame that surrounds each device on both flip-chip

modules. Since the sponsor does not require optimized active surface areas for the mirror surfaces, the frame was inserted to optimize other device characteristics.

As noted in previous chapters, the common bonding frame has demonstrated the tendency to reduce effects of slight bonding errors within the array. The devices within the array typically demonstrate greater uniformity in resting position and actuation characteristics. As shown in Figure 7-8, large bond pads are placed at each corner of the array and smaller pads are placed on the frame surrounding each device.



(a) Actuator receiving module layout

(b) Micromirror host module layout

**Figure 7-8.** Layout of typical cantilever micromirror flip-chip modules.

The bonding of such a distributed assortment of pads tends to produce arrays that are less affected by slight distortions within the array. The probe pads in Figure 7-8(a) are surrounded by a grounded frame to shield each channel from charging effects. The missing surfaces shown in Figure 7-8(b) were intentionally removed to expose the address cell on the receiving module once the array is bonded.

One of the main concerns for any pair of flip-chip modules is the alignment between them once placed in the bonding machine. The two modules shown in Figure 7-8 use an opposing set of asymmetrically distributed pairs of circular and rectangular alignment marks that form the proper pattern in the bonding machine camera system only when the two modules are properly oriented. Since cantilever micromirror devices can only deflect in one direction, the orientation of such arrays is critical. The alignment marks for any flip-chip modules should be designed with adequate spacing between the inner and outer features to indicate rotation errors.

The flip-chip modules shown in Figure 7-8 also illustrate the use of topographically opposed dimpled bond pads to correct for slight alignment errors. Located in the corners of each module, these pads do not support the array, but simply aid in the alignment of the bonding process. The dimples in the host module pads are small bumps while the dimples in the receiving module pads are slightly larger pits that are designed to fit together within 2  $\mu\text{m}$  of lateral error in any direction. These dimples have been shown to correct for alignment errors up to 4  $\mu\text{m}$  beyond the edge of each dimple regions. Therefore, this feature can reduce alignment error from as much as 6  $\mu\text{m}$  to no more than 2  $\mu\text{m}$  during bonding.

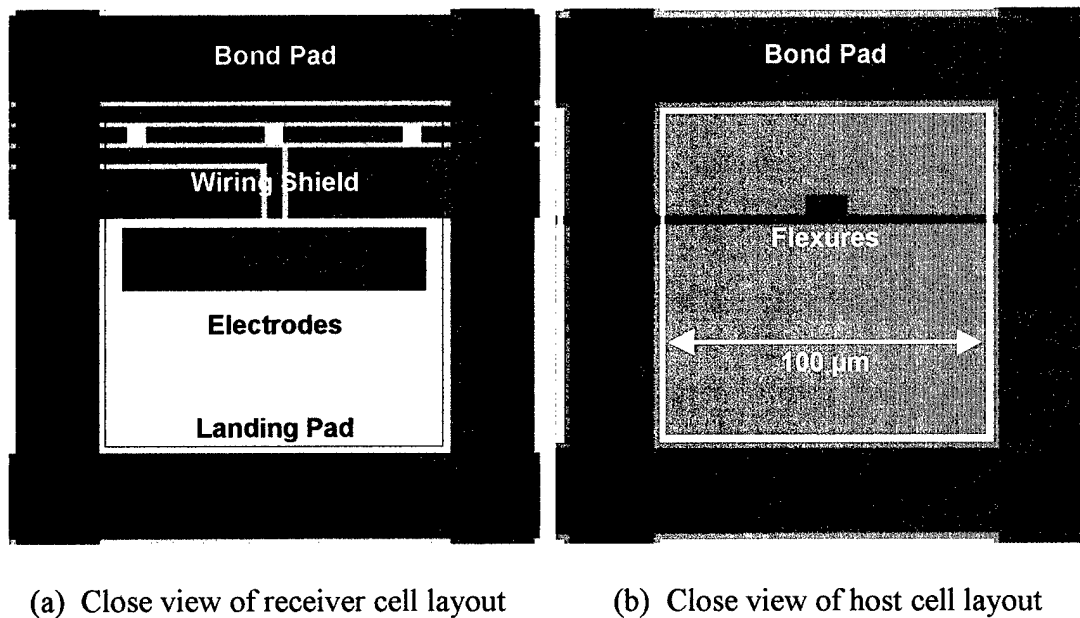
Another optimization enabled by the bonding frame is probably the most useful in terms of bonding yield. Normally, the bonding machine must be repeatedly calibrated to ensure the proper planarity tolerance between the host and receiving module. However, with large bond pads positioned around the edges of the frame and smaller pads within it, the planarity tolerance between flip-chip modules is dramatically increased. For instance, individually bonded devices demand near

perfect planarity between the host and receiving modules since all corresponding pairs of bond pads must be sufficiently compressed to enable the bond. Arrays supported by a common frame, however, require only a portion of the pads to bond. Although it is ideally desirable to securely bond all pads between modules, the entire array can still be supported on the receiving module if only a small fraction of the pads successfully bond. The remaining pads simply rest on gold-to-gold contacts to conduct the ground plane. Such a feature also allows a reduction in the applied bonding force which in turn reduces potential damage to the array.

Another optimization enabled by the bonding frame is electrostatic isolation of each device within the array. Because of the large separation height between the electrodes and the mirror surface, the electric field induced between the plates would normally be distorted along the edges as fringing fields interfere with neighboring devices [24]. Moderate cross-talk effects would likely be observed where resting mirrors would slightly deflect from the plane of the array when adjacent devices are activated. The bonding frames from both modules form grounded walls between devices that span the entire height between the electrodes. As a result, all fringing fields terminate before exerting any extraneous forces on adjacent mirror surfaces.

One drawback to the bonding frame is that the gold pads surrounding each device must be segmented. Previous versions of these arrays had continuous gold bond pads on both the host and receiving modules which formed a continuous wall between the two substrates that was filled with the sacrificial oxide layers of the MUMPs process. As a result, the etch time required to pass HF acid through the entire length of the array was dramatically increased. The enclosed cavity formed

within each device would not begin to etch until the adjacent device had been completely released and gaps in the surrounding walls had been opened. These arrays were more prone to damage during release because of oxide column formation and by the prolonged exposure to acid. Segmenting the bond pads provides an open access to etch all devices simultaneously. Figure 7-9 shows a closer view of the cantilever receiver and host cells illustrating the segmented gold bond pads.



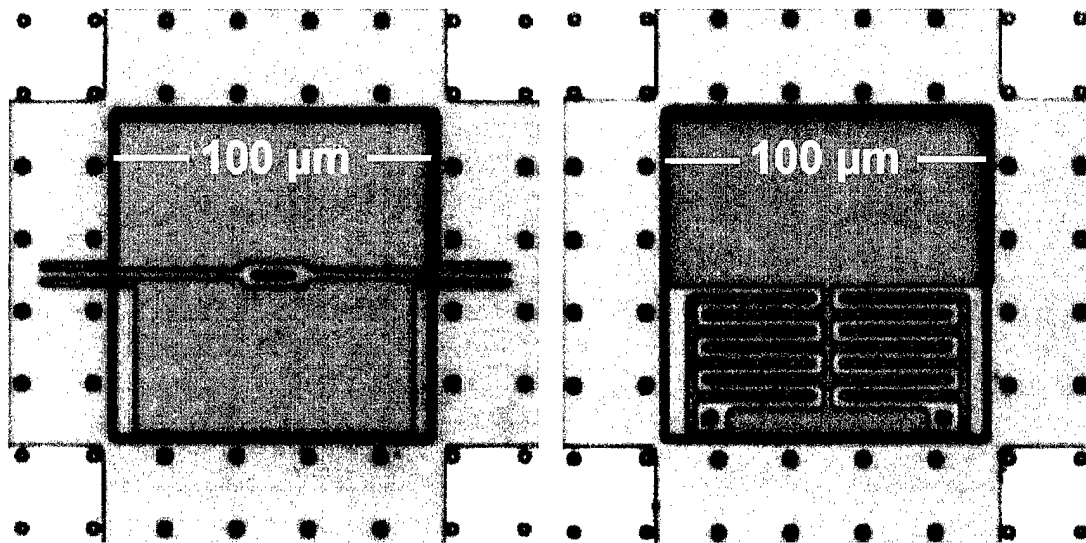
**Figure 7-9.** Layout of typical cantilever micromirror array flip-chip elements.

In addition to grounded bonding columns for electrostatic isolation and segmented bond pads for faster etching, the receiving element in Figure 7-9(a) has several characteristics that have evolved through more than 20 different designs of cantilever micromirror arrays. First, a grounded wiring shield is shown above the address wiring which runs through each device. This shield serves to electrostatically isolate each mirror surface from the various combinations of address signals applied



to the wiring in an attempt to reduce cross-talk effects and variances in actuator performance across the array. Likewise, a grounded landing pad surrounds the address electrode as a stable landing position for the mirror and to eliminate surface charging effects that have been shown to affect neighboring devices within an array. Finally, the elevated address electrode serves to reduce the address potential needed to snap the mirror surface down to a stable resting position.

Although pure torsion flexures like those shown in Figure 7-9(b) allow continuous motion and are most easily modeled, numerous arrays of binary devices were designed with various flexure designs that require a pivot to form a stable resting position. Figure 7-10 shows two such designs employing this feature.



(a) Device with longer torsion flexures

(b) Device with serpentine flexures

**Figure 7-10.** Photographs of flip-chip cantilever devices requiring pivot support.

The longer torsion flexure shown in Figure 7-10(a) is designed to reduce the address potential of the device, but is more likely to deform during actuation such that the

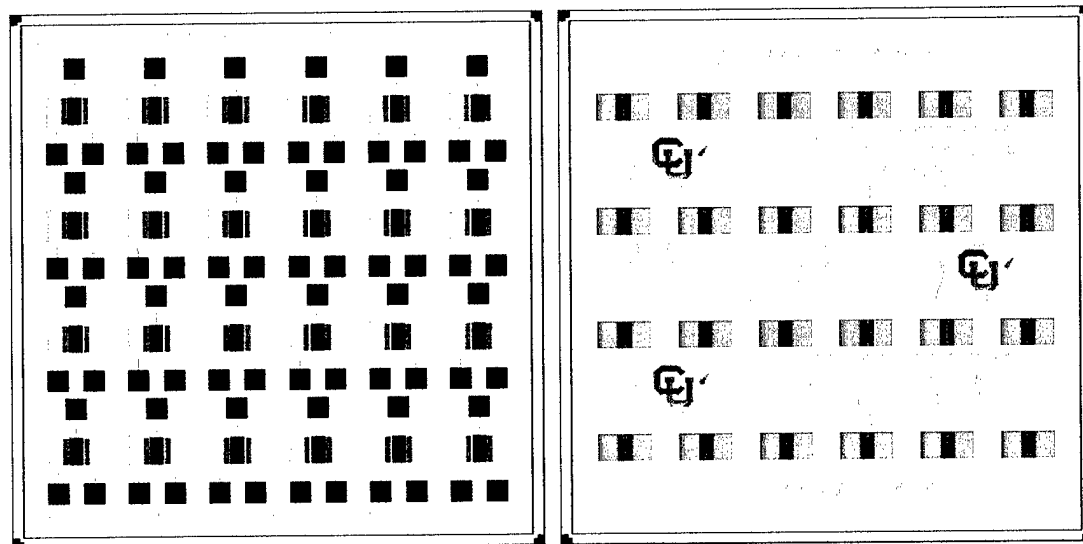
mirror surface will exhibit significant piston motion. Likewise, the serpentine flexure shown in Figure 7-10(b) is designed to reduce the address potential by significantly decreasing the device spring constant. Unfortunately, any attempt to reduce the torsion spring constant in order to lower the address potential will also lower the restoring spring force that is required to prevent piston motion.

Furthermore, the two versions of cantilever devices in Figure 7-10 show that either the micromirror surface or serpentine flexures will be exposed to the address electrodes once bonded. As a result, there is a significant counterforce that acts against the desired motion of the devices and serves to increase the address potential required to activate the device. This counterforce also leads to the piston motion of the mirror surface from the resting position. Because both types of flexures are more susceptible to piston motion, the pivots must be used to prevent the device from collapsing and shorting with the electrodes. Figure 7-1(d) shows such a device in the resting and actuated positions in which the design of the pivot and layout of the mirror surface allow for easy manipulation of the deflected angle of the device.

#### **7.2.4 Design of Torsion Devices**

As previously described, the torsion micromirror devices were simply two cantilever devices mirrored about the axis of rotation to enable deflection along either direction. Therefore, the advances made in the design of the cantilever devices could at any point be applied to a new design of torsion devices should the application for such a device arise. Since the sponsor required only cantilever arrays, very few bi-directional torsion arrays were created as part of this research.

Of the few torsion arrays that were created, some were designed inside a common bonding frame and were virtually identical to many of the cantilever devices except for an opposing electrode on the other side of the device. Other arrays, however, were designed to test the individual bonding approach on devices that experience a torque about the bond pad and could potentially fail accordingly. Since the yield strength of each individual flip-chip bond is subject to countless variables and is essentially unknown, it was desirable to test whether the electrostatic torque designed to actuate the devices could be sufficient to separate bonded pads between the host and receiving features. Figure 7-11 shows two torsion flip-chip modules.



(a) Actuator receiving module layout

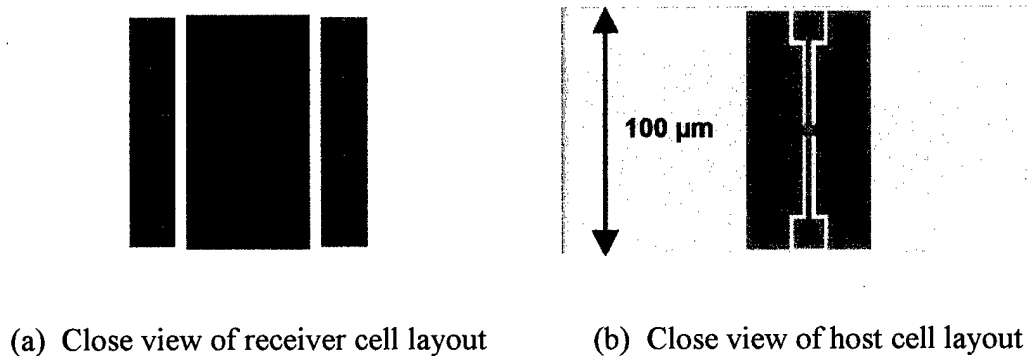
(b) Micromirror host module layout

**Figure 7-11.** Layout of individually bonded torsion micromirror flip-chip modules.

The devices within the array are individually bonded and are also individually probed to test the actuation of the devices while ensuring that other devices were not accidentally actuated and destroyed. The bond pads are designed to be much taller

than wide so that any orthogonal rotation between the two modules would be easily noticeable under the bonding machine camera system. The two modules were designed to be symmetric about the other axis so that the proper alignment could be achieved even if one module were rotated relative to the other.

Similar to the polar piston array, the individual  $50 \times 100 \mu\text{m}$  bond pads were designed to be large enough to compensate for any lateral alignment error. The bond pads are shown in Figure 7-12 which illustrates the design of each flip-chip element.



**Figure 7-12.** Layout of typical torsion micromirror array flip-chip elements.

The torsion flexures of the device are fabricated in the same layer as the host bond pad shown in Figure 7-12(b) in which the bond pad is segmented into two portions. Both segments are intended to bond with the larger bond pad in Figure 7-12(a) in the center of the receiving cell. Again, the receiving bond pad is designed with spacer layers beneath it to ensure it is the tallest feature on the receiving module. Similar to many of the cantilever designs, this torsion device uses the elevated address electrodes to reduce the address potential and a grounded shield and landing pad surrounding the electrodes and bond pad of the receiving cell.

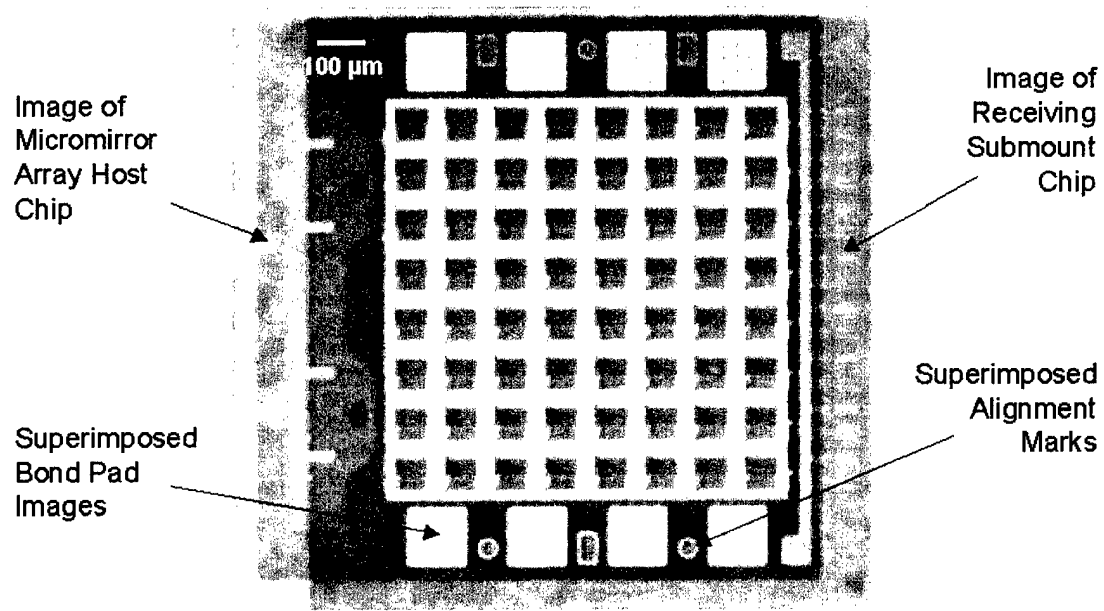
### **7.2.5 Assembly of Flip-Chip Modules**

Most of the procedures necessary to perform submount flip-chip assembly are very familiar to MUMPS designers. There are only a few simple steps added to the normal procedure for the release and testing of a typical MUMPS chip. First, each of the 1 cm square chips delivered from the foundry is diced into as many as 100 much smaller flip-chip modules. This allows for as many as 50 flip-chip arrays from each of the 15 delivered MUMPS chips per fabrication run. Although an older dicing saw has been used at the University of Colorado, far better results are regularly obtained using any one of a number of commercial dicing services.

Once diced and sorted, the flip-chip modules are initially soaked in Acetone for roughly 20 minutes to remove the outer layer of packing photoresist that is designed to protect the devices during shipping and dicing. The modules are then rinsed in Methanol for another 15 minutes to clean any remaining material that may contaminate the bonding process. Immediately prior to bonding, the flip-chip modules are cleaned for one minute in 25-watt argon plasma to remove any loose debris or material that would otherwise interfere with the bonding of gold surfaces. For thermo-compressive or thermo-sonic bonding between MUMPS submount modules, no other preprocessing steps are necessary.

As described in Chapter 4, the custom-built flip-chip bonding machine is used to invert and align the host substrate to the receiving substrate in preparation for bonding. As previously described, the resolution of the camera system used to align the opposing modules is not sufficient to discriminate between smaller features such as flexures or address wires on either module. Therefore, the larger alignment marks

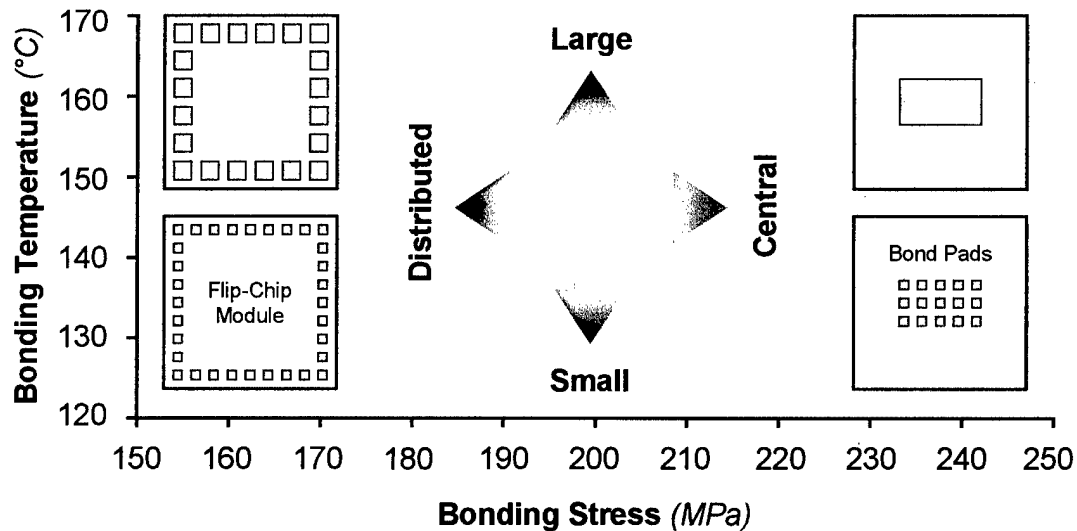
are designed and placed on the two modules to allow for proper alignment between the features in the receiving cell and the host cell within the arrays. As previously described, the orientation of the two modules is critical for the proper operation of cantilever devices, so these alignment marks must be asymmetrically distributed to clearly indicate improper orientation. Figure 7-13 shows the superimposed images of these alignment marks as viewed in the bonding machine.



**Figure 7-13.** Image of superimposed cantilever micromirror flip-chip modules.

The smaller features drawn on the receiving module are designed to fit within the larger features drawn on the host module. Sufficient space is allowed between them in order to indicate any rotation error between the two modules. Also shown in Figure 7-13 are the bond pads that are distributed around the edge of the bonding frame. The superimposed images of these pads clearly show topographically opposed dimples that are designed to reduce alignment error during bonding.

Once properly aligned, the bonding machine camera system is removed at which point the gold layers between the modules are bonded at elevated temperatures. Both the bonding temperature and applied bonding stress seem to depend on the size and distribution of the bond pads around the modules. A recommended range of each parameter was determined purely by qualitative observations of literally hundreds of submount flip-chip bonds. Figure 7-14 illustrates this relationship between the bonding temperature and applied bonding stress versus bond pad configuration.



**Figure 7-14.** Plot of bonding temperature and stress for bond pad configurations.

The lower bonding stress is recommended for distributed bond pads since even slight planarity variances between modules can fracture the structures along one side of the modules while the features on the other side do not bond. In this case, a lower bonding stress is simply a precaution to prevent damage to the modules. Centrally located pads are less affected by such variances and can typically bear a greater load.

Additionally, larger pads seem to bond more reliably at much higher temperatures. Unfortunately, some adverse bonding effects become noticeable at higher temperatures. For instance, any enclosed cavity within the devices can reduce bonding yield if the flip-chip modules are joined too quickly such that the air trapped between them is not allowed to expand and escape prior to bonding. To reduce this effect, the flip-chip modules can be held in close proximity and allowed to slowly reach the bonding temperature before they are slowly brought into contact.

Finally, the bonded modules are released in a standard 48% HF etch to remove the oxide layers between them, dispose of the micromirror host substrate, and free the structural layers of the flip-chip device. Extra care must be taken to avoid damage to the arrays if any agitation is used during release. The etch time varies for different designs of arrays depending on cavities formed within the devices.


### **7.3 Yield Analysis**

One primary concern regarding submount flip-chip fabrication is the yield of the entire process. Since the bonding machine is for group use, it is often out of alignment and must be calibrated for alignment and planarity between applications. Additionally, the quality of the MUMPS features, the outgassing of enclosed cavities during bonding and the adverse chemical and mechanical effects observed during release tend to lower the process yield. If a reasonable attempt is made to counter or avoid these effects, the yield can be dramatically improved and has typically exceeded 80% when the bonding machine is precisely calibrated between each bond.



Over the last two years, a variety of flip-chip bonding techniques have created a performance history that can be studied to determine which technique or design features work best in this process. In order to do so, a complete yield analysis was performed on all fabrication procedures related to the standard thermal-compression bonding process involving the use of opposing submount modules. Table 7-2 shows the resulting yield for each step in the flip chip process spanning several MUMPs fabrication runs. Only those lots in which sufficient samples of flip-chip modules were fabricated are included in the analysis.

**Table 7-2.** Comparison of yield for each step in the flip-chip assembly process.

MUMPs:	33	35	38	39	40	41	42	Typical Failure Mechanisms:
Design:	100	100	95	100	100	100	90	Poorly Copied or Placed Cells, Poor Design and Fabrication Assumptions
Fabrication:	100	100	98	100	100	3	100	Ultrasonic Damage, Overetching, Photolithographic Pattern Errors
Dicing:	96	100	100	94	100	100	100	Poor Alignment, Chipping
Cleaning:	100	87	100	100	96		100	Overexposure Damage to Fine Features
Bonding:	38	45		75	72		88	Poor Alignment or Module Planarity, Fractured Features
Release:	50		25		46			Separation, Oxide Columns, Contamination, Galvanic Cell Damage
Drying:	100	94	85	96	100		100	Contamination, Debris, Tumbling Damage
Testing:	100	100	100	94	100		96	Localized Probe Damage, Shorting of Individual Devices
Handling:	100	98	100	98	100		100	Chipping, Module Separation, Positioning Errors
Total (%):	18	22	13	36	32	3	41	0%  100%

The numbers given in Table 7-2 do not represent absolute yield for the entire process since some modules were not used in all steps of the flip-chip assembly process. For

instance, all flip-chip modules are fabricated and diced, but some of those are never bonded. The yield for each section of the process in Table 7-2 is shown only for those modules exposed to that processing step. The total yield is extrapolated using these values to indicate the expected yield if all fabricated modules were subject to the entire flip-chip fabrication process.

It should be noted that this method tends to hide advances in one phase of the process or in one style of device. For instance, some arrays are designed with a large individual bond pad to reduce alignment errors. The yield for these arrays is much greater than others, but the total yield for that run is reduced by poor performance from other devices. In this manner, the flip-chip bonding technique can often appear to be prone to failure when, in fact, some devices are unprecedented achievements.

For the purposes of this analysis, a failed flip-chip module is defined as one in which any single critical component was damaged to the extent that the entire module as a whole did not operate as designed. For instance, if a single address wire running to one micromirror within an array is damaged, that device is not functional and the entire array is considered to be lost. Some perfectly bonded arrays have been considered lost as a result of holding the module with tweezers. If small chips or cracks along the edge of the module prohibit even a single wire bond or probe tip connection, the entire array becomes flawed and is therefore counted as a failed module under the handling process. Also for the purpose of this analysis, a process failure in any step of the complete flip-chip assembly process was considered a critical failure. Although the module itself may have undergone further testing, the yield is calculated such that no failed module was counted in more than one step.

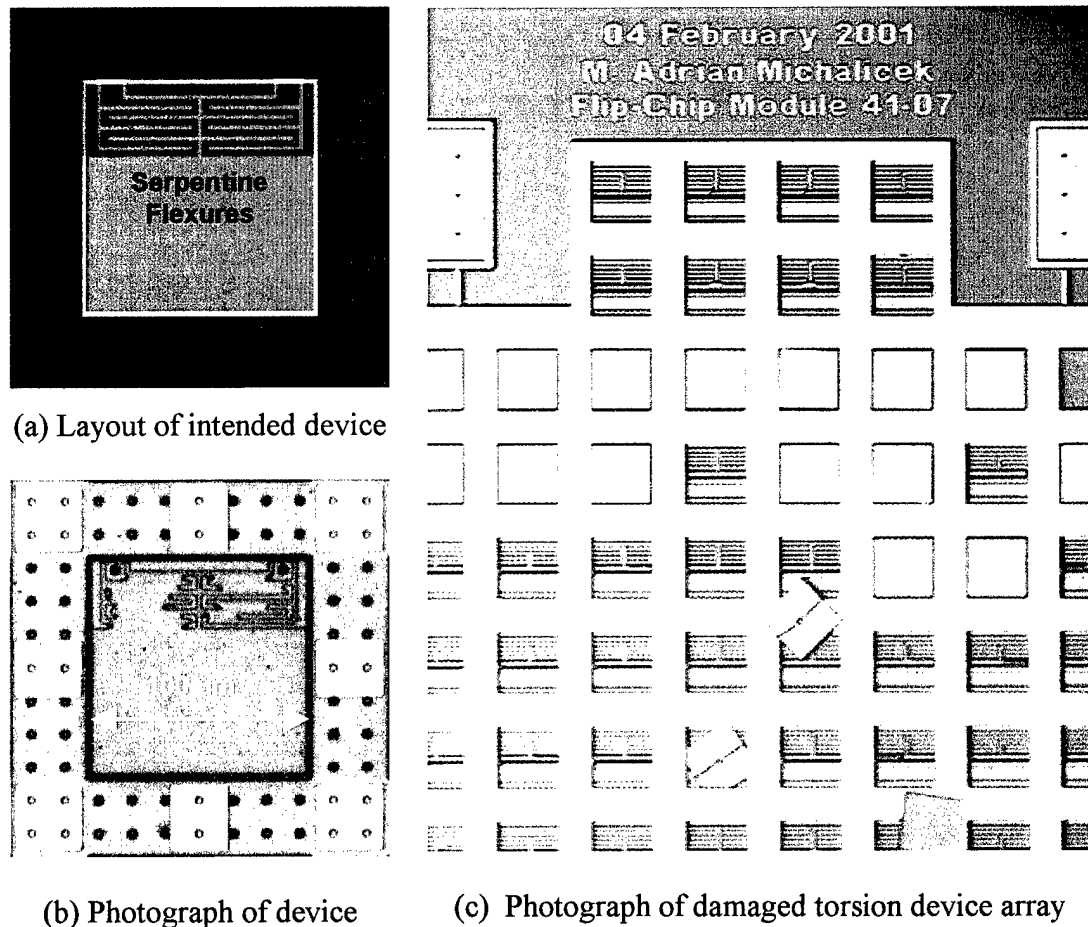
Devices that displayed adverse characteristics yet were still functional were not counted as failed modules. For instance, some arrays created in MUMPs 38 were bonded atop receiving modules that did not include a grounded landing pad within each device or isolation plane surrounding each address electrode and probe pad. As a result, the devices displayed very slow switching frequencies and severe cross-talk interference from surface charging of the isolation layer on the receiving substrate. Although these devices displayed unfavorable behavior, they consistently deflected as designed and were therefore considered to be successfully assembled.

As noted in Table 7-2, the bonding yield has dramatically increased due to improved calibration of the bonding machine and better design techniques resulting from observing early failure mechanisms. Flip-chip structures are now designed with features to increase alignment tolerance and reduce stress concentration damage during bonding. For instance, the use of large individual bond pads on polar piston micromirror arrays has demonstrated the best bonding yield to date.

### **7.3.1 Commercial Prefabrication Errors**

Unfortunately, as noted in Table 7-2, some of the single worst cases of lowest yield involve critical failure mechanisms that are simply not in the control of the designer. For instance, the entire lot of MUMPs 41 modules was lost due to fabrication errors at the commercial foundry. None of the delivered features produced working devices. An initial inspection of the delivered modules showed obvious damage to fine features such as the flexures that support the mirror surfaces within the array. Most of the flexures were malformed or simply missing.

A layout of the intended cantilever device is shown in Figure 7-15(a) in which two serpentine flexures support the mirror surface. Although these flexures were created within the design rules for the MUMPs process, the resulting array shown in Figure 7-15(b) clearly illustrates prefabrication damage as the array is still packed in protective photoresist as delivered from the foundry.



**Figure 7-15.** Illustration of commercial prefabrication errors and resulting array.

The foundry service eventually confirmed that malformed features were the result of ultrasonic damage. Although every module from this lot was considered a fabrication

loss, some modules were bonded to test the limits of the bonding force profile. As shown in Figure 7-15(c), nearly all of the torsion micromirror devices within the arrays literally fell apart during release. Most of the devices that survived the bonding and release process quickly failed when activated during testing.

### **7.3.2 Flip-Chip Module Planarity**

Many of the diced modules that were prefabricated in the MUMPs process have demonstrated significant planarity variances between modules. Two opposing flip-chip modules intended for bonding in the flip-chip bonding machine are assumed to be perfectly planar between the front and back of the modules. Since the modules rest on the stage and horn during bonding, any deformations in either surface of the modules will affect the mating of opposing flip-chip bond pads.

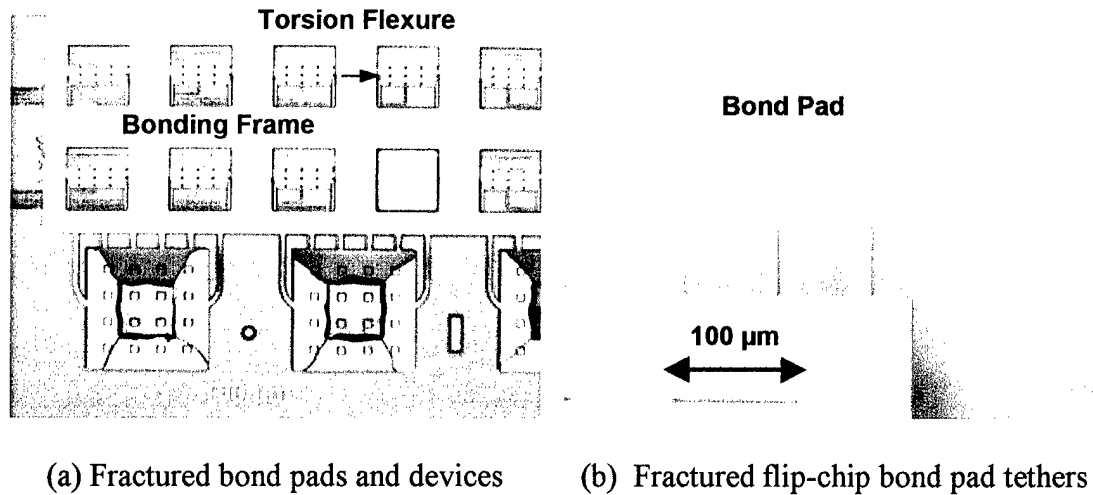
The same Zygo interferometric system typically used to test the performance of micromirror devices was used to test the planarity of a large sample of flip-chip modules. Surprisingly, some of the 2 mm square flip-chip modules demonstrated as much as  $0.04^\circ$  of surface tilt relative to the back of the module. If the direction of this tilt is parallel to the axis about which host modules are inverted relative to the receiving module, then any given pair of flip-chip modules could possibly have an angle of  $0.08^\circ$  between mating surfaces. In short, when one side of the 2 mm square modules makes contact, the other side could still be separated by as much as a  $2.8\text{ }\mu\text{m}$  gap. Such a gap would prohibit bonding along that side of the module and may cause damage to those pads in contact if too much bonding force is applied.

Although this is clearly the worst possible case of the observed tilt, many arrays of individually bonded devices have demonstrated a bonding threshold between regions where all devices bonded and others where no devices bonded. Many of the devices that failed to bond had no indentations in the bond pads which indicates that the opposing gold features simply did not make contact with sufficient force to form the bond. Furthermore, if a randomly chosen host module intended for calibrating the bonding machine demonstrates significant planarity error, the bonding machine could erroneously be calibrated to an angle at which all subsequent flip-chip modules fail to bond.

### **7.3.3 Fracture of Flip-Chip Structures**

Using the standard thermo-compression flip-chip bonding process, flip-chip structures are bonded to receiving cells while both are still encased in oxide layers. Although it is easy to assume that these features are highly rigid, many arrays have shown that critical structures can fracture if too much bonding stress is applied. Although the target bonding stress for typical submount flip-chip modules is roughly 150-250 MPa at 170°C for larger bond pads, it should be noted that some arrays have been damaged when planarity issues limit the contact between modules to only a few bond pads or devices within the arrays. Figure 7-16(a) shows one such array in which a small number of bond pads and mirror surfaces on one side of the host module were subjected to the entire bonding force. The host bond pads on the opposite side of the array and the majority of support frame pads within the array did not make contact

with the receiving pads. As a result, the few bond pads that did make contact fractured under the load that was effectively four times the intended bond force.



**Figure 7-16.** Photographs flip-chip structures fractured during flip-chip bonding.

The array shown in Figure 7-16(a) consists of cantilever micromirror surfaces supported by a pair of pure torsion flexures. A portion of one such flexure is still visible. The four bond pads nearest the contact edge of the flip-chip modules have fractured and the flexures of all but one device along that edge have been destroyed. Although the bonding force could be reduced to a level where the risk of such damage is minimal, doing so increases the number of arrays that simply do not bond. As a result, roughly 10-15% of flip-chip arrays show some signs of fracture damage or incomplete bonds.

In addition to accidental damage from planarity errors, some early arrays demonstrated fracture damage to key features that were simply designed with sharp corners and other stress concentration points. These points simply failed during

bonding when higher bonding forces were required to secure the flip-chip structures atop the receiving module. The bond pad tethers in Figure 7-16(b) simply broke at the base of the bond pad where they were poorly connected between structural layers with sharp angles. The topography and shape of the connections made them the weakest point within the array. Later arrays were designed with features that dramatically reduce stress concentration points around the pads.

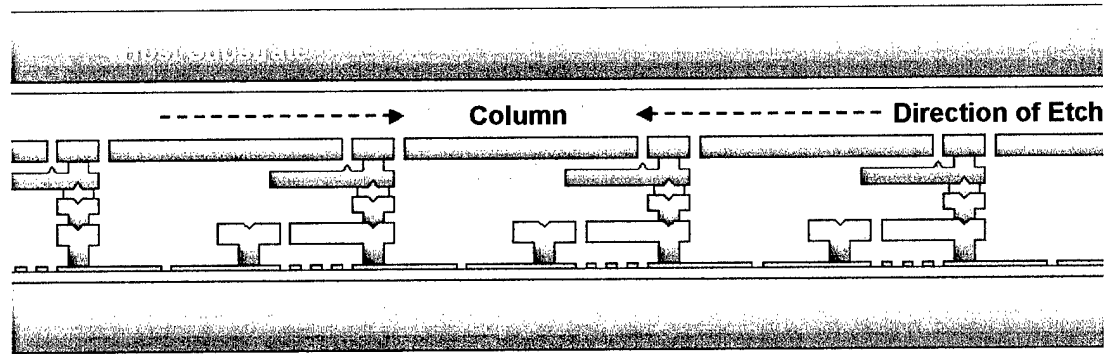
#### **7.3.4 Oxide Column Damage**

Perhaps the most destructive portion of the flip-chip bonding process is the release etch that frees the flip-chip structures and removes the spent host substrate. A number of adverse chemical and mechanical factors pose a threat to the arrays, but the most consistent and potentially damaging is the formation of oxide columns between the mirror surfaces and the host substrate as the oxide is etched between the modules. Early designs of micromirror arrays had continuous gold surrounding each device within the array. When this gold bonded, the volume within each micromirror device formed a closed cavity that could not be etched until the HF solution had etched through an adjacent device. As a result, small columns of oxide formed in the center of the flip-chip modules since those devices did not begin the etch process until well after the devices around the edge of the module had been released.

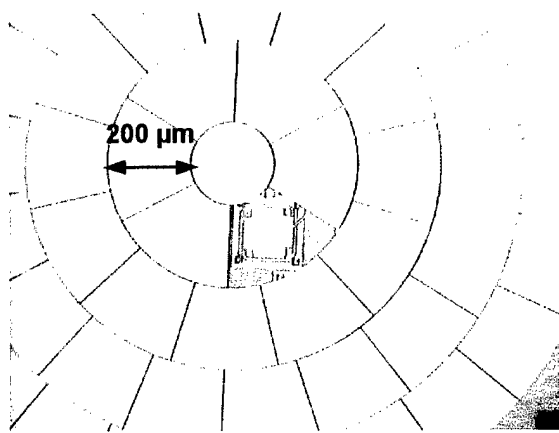
The formation of oxide columns poses a significant threat to mirror surfaces at the center of the arrays because the same compliant flexures that enable the devices bear the entire load of the host substrate if the mirror surface remains connected to it by such a column. Figure 7-17(a) shows a cross section of a typical bonded



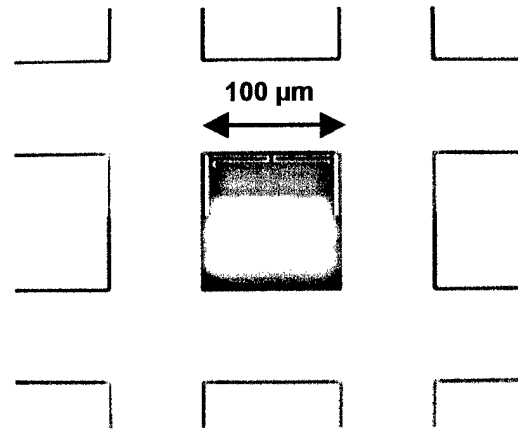
cantilever array during the release etch in which the host substrate is almost completely released. The formation of the final oxide column above a single micromirror device threatens to strip that surface from the array if the solution is agitated or disturbed in any way.



(a) Cross-section of a typical flip-chip cantilever array showing oxide column.



(b) Damaged polar piston array



(c) Damaged cantilever array

**Figure 7-17.** Illustration of typical oxide column damage to flip-chip arrays.

The array shown in Figure 7-17(b) is typical of arrays that are nearly released when some slight agitation disturbs the host substrate which literally rips the attached mirror surface from the array. Although all other devices within the array work as

designed, this array obviously represents a failed module and reduces the yield of the release process. Likewise, the cantilever array in Figure 7-17(c) demonstrated similar oxide column damage and shows remnants of the serpentine flexures that are left after the mirror surface was pulled from the device.

Unfortunately, many host modules can be completely released, but remain positioned directly over the receiving module in the release solution. Quite often, a slight agitation is required to simply identify the arrays to be removed from the solution. To improve the release yield, the relative etch rate is determined for all arrays based on geometry and the amount of exposed oxide within the devices. The etch rate is used to determine the expected amount of time required to release the array. A safety margin is added to that time during which the solution remains completely undisturbed. Although many arrays will rest in the release etch for longer than necessary, the average amount of damage caused by oxide columns has dramatically decreased with recent flip-chip modules.

### **7.3.5 Galvanic Cell Damage**

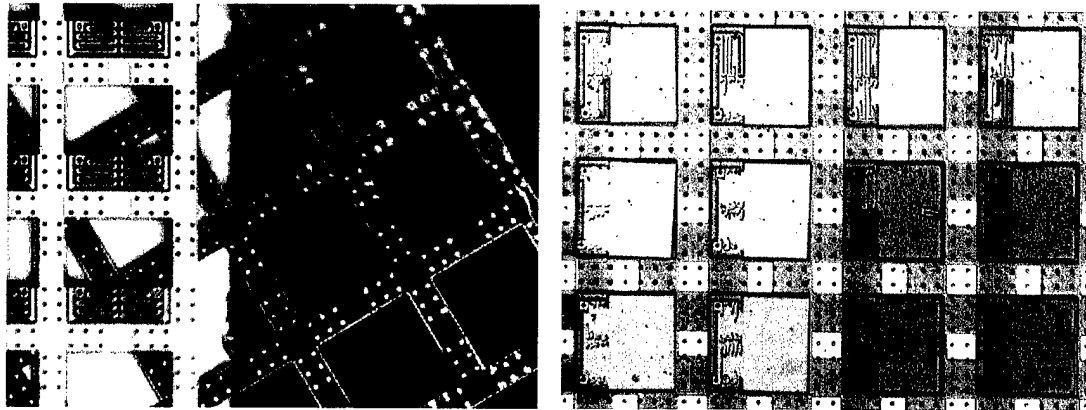
Another potential cause of the delayed switching of these type of devices is the electrolytic effect observed during the release etch. Some arrays have gold covering more than 70% of the surface area on the inside of both chips. While submerged in 48% HF acid during release, a current is produced through the structures which appears to selectively etch locally doped regions of polysilicon leaving porous silicon address wires. Resistivity measurements of address wires in excess of 100 k $\Omega$  have been observed in extreme cases. Second generation devices

employ minimal gold bonding areas and, together with a modified release procedure, have eliminated the effect.

Because the flip-chip assembly process relies on large quantities of the gold layer of the MUMPs process, many flip-chip structures have demonstrated some degree of discoloration or other adverse electrochemical effects during release. In extreme cases, some devices have been reduced to porous polysilicon in which mirror surfaces become transparent and flexures become quite brittle. In many cases, the resistivity of address lines supplying the devices increases so much that higher frequency testing of the devices is not possible [21]. Prior to release, some mild damage and discoloration is already visible from the foundry processing of the gold layer atop polysilicon features. Polysilicon probe pads connected to features with sufficient gold area typically appear darkened upon delivery from the foundry.

The damage results when a galvanic cell is formed in the HF solution where the exposed polysilicon and gold act as a local anode and cathode, respectively [25]. Silicon atoms are oxidized by two valence band holes and dissolve into the solution as a fluoride complex. The level of damage is proportional to the relative current between the nodes and is a function of numerous variables such as HF concentration, the presence of oxidizing contaminants, addition of surfactants, illumination, area of exposed polysilicon and gold, polysilicon resistivity, and etch time. Unfortunately, this galvanic effect has been reported in a 1% HF solution which is well below the concentration typically required to release the MEMS structures [25]. Therefore, other variables must be manipulated to reduce the effect.

The arrays shown in Figure 7-18 illustrate extreme cases of the galvanic effect. Although the arrays in Figure 7-18 were prereleased for integration atop CMOS receiving modules, a similar but lesser degree of damage is often observed in arrays that are flip-chip bonded atop other MUMPs receiving modules.



(a) Separated bonding frame

(b) Selective mirror surface damage

**Figure 7-18.** Photographs of extreme galvanic cell damage during release etch.

The bonding frame surrounding most devices consists of both upper layers of the MUMPs process connected by distributed pairs of “via” cuts between them. As shown in Figure 7-18(a), however, these layers have separated after the galvanic effect has dissolved these connections. The highest dopant concentrations in these structural layers is located along the surface of the frame. As a result, the galvanic effect has attacked and discolored the lower polysilicon frame and destroyed the via cuts at the interface between the two layers. Likewise, the mirror surfaces are released from the via cuts at the ends of the flexures.

The damaged array shown in Figure 7-18(b) offers unique observations in the study of this effect. This array was part of the lot that was subject to fabrication errors at the foundry. The serpentine flexures within each device are clearly marred by ultrasonic damage which resulted in portions of the flexures breaking away. As a result, only some devices within the array maintain an electrical contact with the support frame on which the gold bond pads are distributed. During the release etch, those devices in which both serpentine flexures fractured are isolated from the effect and appear lighter in color as they were not damaged. Other devices, however, in which at least one flexure remained fully formed were still connected to the frame and were then stripped of silicon atoms forming a porous mirror surface. Many of the devices in Figure 7-18(b) display portions of flexures that fall into both categories and therefore appear as two distinct colors.

Another interesting observation is the fact that loose portions of polysilicon adhere to nearby features during the release etch in proportion to the level of galvanic damage. Although the released mirror surfaces shown in Figure 7-18(a) are completely free of the flexures and support frame, they remain in place as they are now bonded to the surface of the isolation layer on the substrate. Likewise, small pieces of damaged flexures in Figure 7-18(b) are bonded to mirror surfaces. Even those features electrically isolated from the galvanic effect are subject to the enhanced stiction. Many of the isolated mirror surfaces in Figure 7-18(b) are slightly rotated relative to the support frame, but can only be removed from the surface of the substrate when stripped with a probe tip. This effect in particular has moderately

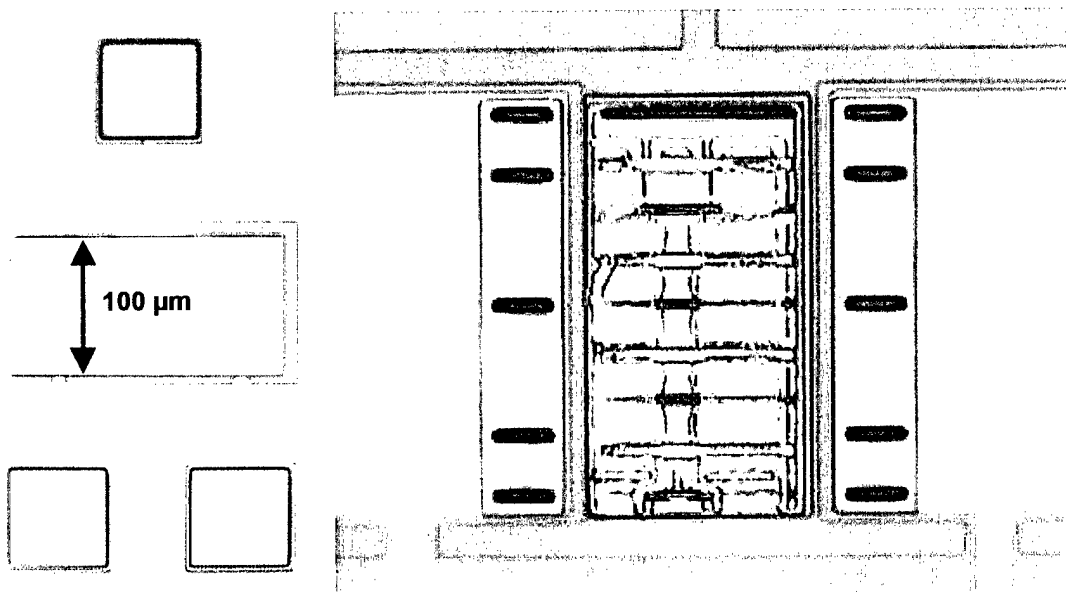
reduced the yield of integrated micromirror arrays that are released prior to flip-chip bonding atop CMOS receiving modules.

Although inconsistent with the proposed structure and behavior of the galvanic cell, the damage also appears to be enhanced when multiple flip-chip modules are released in close proximity within the HF solution. Damage to micromirror arrays released individually was undeniably less than identical arrays fabricated in the same MUMPs lot that were released in large quantities. Since the absorption of oxidized silicon ions into the solution produces large quantities of free hydrogen ions required to oxidize additional silicon atoms, it is likely that the close proximity of the flip-chip modules sustains a higher rate of the reaction.

A number of techniques have been attempted to minimize this galvanic cell damage during release. First, the addition of a surfactant has slightly diminished the extent of the damage, but also increased the etch time required to release the arrays. As a result, the released arrays show moderate adverse characteristics related to prolonged exposure to the HF solution. Another technique involves the isolation of the solution from light sources. Reports of similar observations have determined that illumination is required to generate valence band holes in n-type silicon to enable the galvanic cell [25]. Unfortunately, all attempts to isolate the release solution from light sources have shown to be largely ineffective in reducing the damage. At present, this effect appears inconsistent between flip-chip modules fabricated in different lots of the MUMPs process which might suggest that the extent of the damage varies by doping concentration or other process variables that are not available for modification by the designer.

### 7.3.6 Bond Pad Compression

A typical torsion device is shown in Figure 7-19(a) which shows a slight misalignment of roughly  $3\text{--}4\text{ }\mu\text{m}$  to the lower left of the image. These devices can tolerate up to  $30\text{ }\mu\text{m}$  of alignment error using a single large bond pad in the center of the device to support the mirror surface atop the receiving bond pad. Although most of the torsion devices were successfully bonded to the receiving module, virtually none of the devices demonstrated proper deflection behavior.



(a) Bonded device

(b) Exposed bond pad of separated torsion device

**Figure 7-19.** Photographs of a failed flip-chip torsion micromirror device.

After observing that few of these devices activated, several mirror surfaces from devices with the worst case alignment error of  $8\text{ }\mu\text{m}$  were removed to reveal the receiving bond pads of the device. Figure 7-19(d) shows one such pad in which indentations can be seen where the flexures and mirror posts were embedded in the

gold of the receiving bond pad. At the time of design, it was not yet known that the gold layer of smaller bond pads compresses more significantly under the same bonding stress than the larger pads that have been regularly used. The typical clearance of 0.5  $\mu\text{m}$  from the flexures and posts to the surface of the gold on the host bond pad was erroneously assumed to be sufficient to allow for complete motion of the mirror surface. As a result, this array of devices was considered a design failure.

### **7.3.7 Bond Pad Contamination**

Several bonding experiments were conducted to determine the bond strength as a function of temperature and bonding force for various sizes and geometric shapes of bond pads. Two different experimental pull-testing systems were used to determine the bonding strength of a special set of flip-chip modules designed with bond pads of varying sizes and shapes. Although the quantitative results varied between the two systems, there was one observation that remained consistent between all tests. Those modules that were plasma cleaned prior to flip-chip bonding demonstrated significantly greater bond strength than identical modules that were not similarly prepared. In almost all cases, the force required to break the bonds between the plasma cleaned test modules was roughly four or five times greater than the control modules. Similarly, modules prepared with plasma cleaning also demonstrated a higher bonding yield during the test than identical modules that were not prepared. Ultimately, all modules intended for flip-chip bonding should be plasma cleaned immediately prior to bonding.



## 7.4 Device Performance

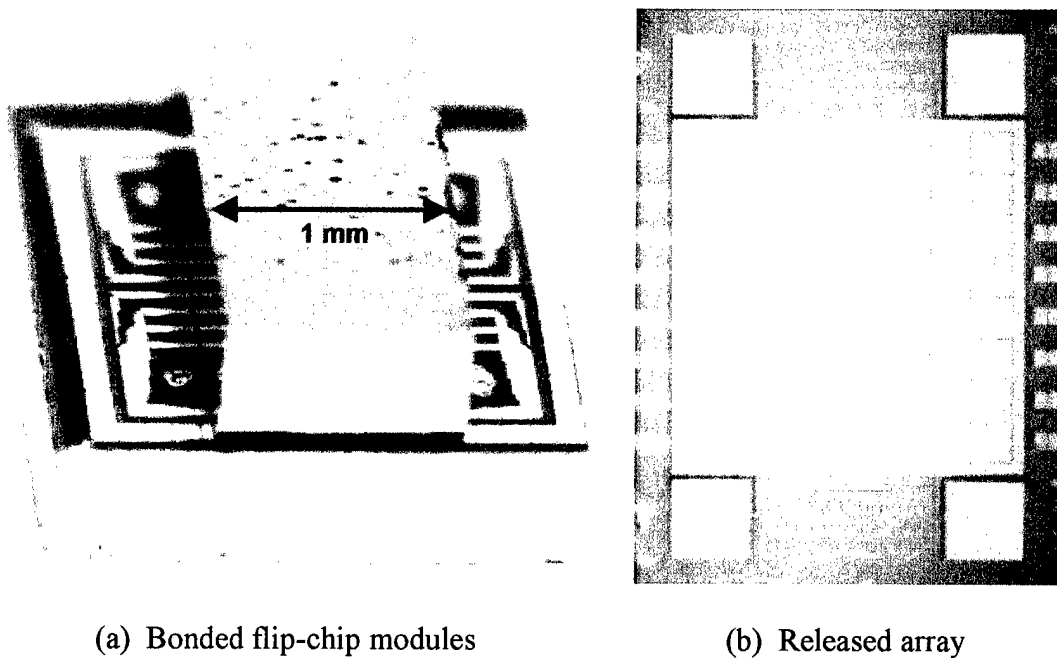
As with other forms of flip-chip bonding presented in other chapters, the submount flip-chip devices were characterized for both bonding quality and final device behavior. This section describes the performance of typical piston and cantilever micromirror arrays and includes any desirable or adverse bonding characteristics demonstrated by the devices as well as surface deflection data.

The micromirror arrays were tested using a Zygo interferometric microscope to determine key features of the arrays and to characterize individual micromirrors. The measuring system sweeps an interferometric intensity pattern across the surface of the array and then calculates the relative deflection of each portion of the array based on the intensity at that position. A three-dimensional image of the resting and activated micromirror device can be generated from this data. This system provides a cross-section tool to obtain a deflection profile along any line drawn through a surface plot and several caliper tools to obtain precise position and angle measurements at any desired point along the characterized surface.

Using these tools, the deflection or tilt of any mirror surface can be accurately quantified as a function of the address potential applied to the device. Additionally, critical micromirror characteristics like planarity and roughness can be measured across the entire surface with better than 1 nm of precision. This system was used to characterize the deflection of piston devices and the tilt of cantilever devices as well as gather surface roughness and array planarity data.

#### 7.4.1 Bonding Characteristics of Piston Arrays

As previously described, the original piston flip-chip micromirror arrays were a surprising success which spawned numerous design iterations and more advanced piston arrays. Figure 7-20 shows photographs of two bonded flip-chip modules and the final micromirror array after release.

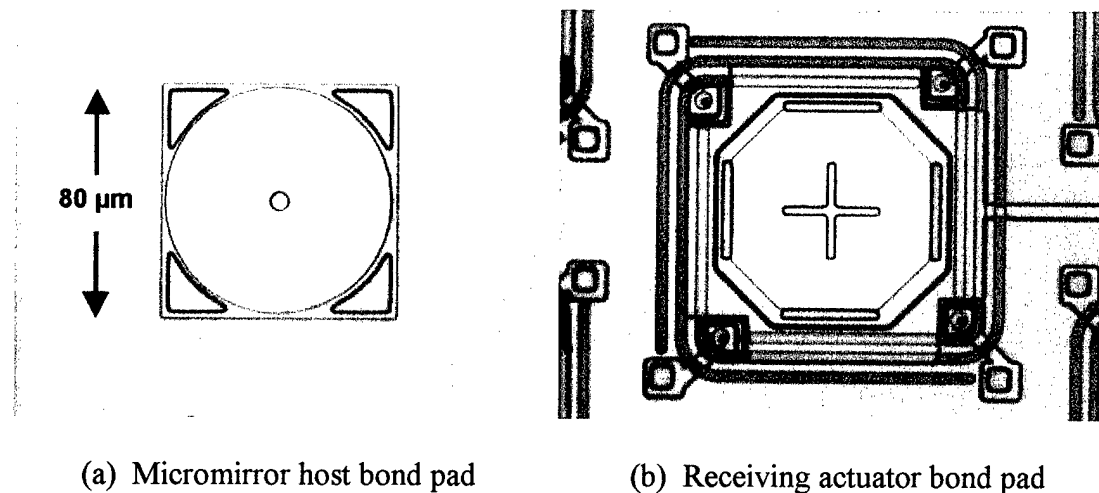


**Figure 7-20.** Photographs of an early rectangular piston flip-chip micromirror array.

The two flip-chip modules shown in Figure 7-20(a) were bonded only by the gold layers available in the MUMPS process. No additional adhesive material was used. Figure 7-20(b) shows a typical rectangular piston micromirror array boasting 98% active surface area since the flexures and other support structures are hidden beneath the planarized surface. Most of these arrays showed very little variance across the surface of the array or distortions in the bonding frame between adjacent devices.

Flip-chip micromirror arrays of this type are also inherently ready for post-process metallization if a specific reflective material is desired. The underlying layers of the receiving chip are almost always shielded from the gaps in the mirror surfaces. Therefore, a simple post-process deposition can be used to cover the mirror surface with a reflective material while avoiding shorts in the address wiring beneath each device [26]. This capability has been demonstrated with similar arrays [27].

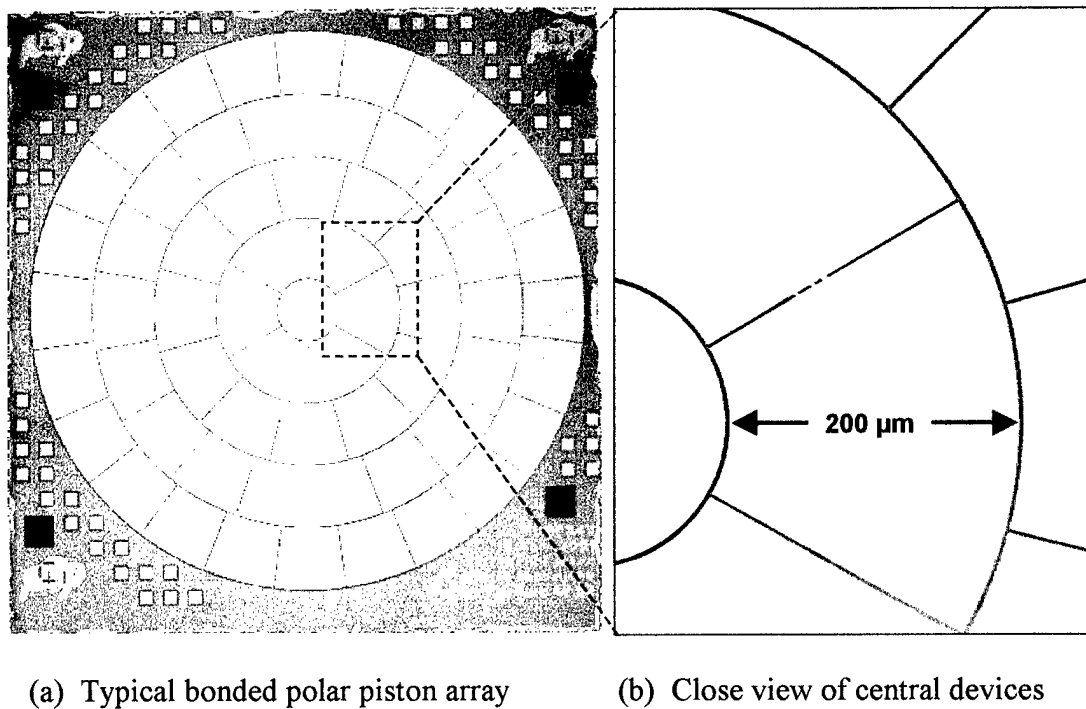
Like the rectangular piston arrays, the polar piston micromirror arrays were also a surprising success. The individual 80  $\mu\text{m}$  bond pads from both modules are shown in Figure 7-21(a) which also shows small features carved into the surface of the gold used for fine alignment. Although these devices were designed to tolerate as much as 40  $\mu\text{m}$  of alignment error, no array showed more than 6  $\mu\text{m}$  of misalignment.



**Figure 7-21.** Photographs of bond pads within the polar piston micromirror array.

Once bonded, a visual inspection of the polar piston micromirror arrays shows that nearly all arrays bonded with minimal alignment error. Although the typical

yield for flip-chip micromirror arrays is notably lower, these arrays demonstrated greater than 73% yield throughout the entire submount flip-chip assembly process. That is, of the original 15 sets of flip-chip modules fabricated in the first batch, there were 11 final arrays that were fully formed with all devices securely bonded and actuating normally. Figure 7-22 shows two photographs of a typical polar array.



**Figure 7-22.** Photographs of a typical released polar piston micromirror array.

Of the arrays that failed, three of the remaining four failed only by a single device in the center of the array that was damaged during the release etch. The nature of micromirror arrays makes them somewhat difficult to fabricate using the flip-chip assembly method. The mirror surfaces must be supported by thin flexures in order for the devices to activate, but those same flexures bear the load of the entire host

substrate during release as oxide layers are etched down to small columns between the mirror surfaces and the host substrate. As a result, any motion during certain periods of the release process will literally rip a few central devices from the array.

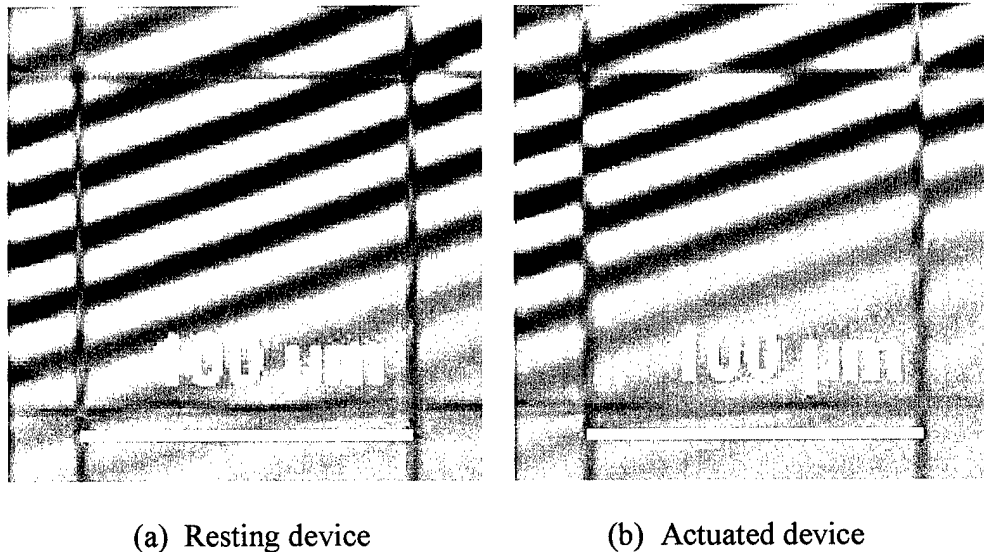
Once bonded and released, a final array is shown in Figure 7-22(a) which illustrates some of the benefits of the flip-chip assembly process. These advanced arrays are planarized with five structural layers and boast more than 98.3% active surface area. The fast etch rate of the MUMPs oxide along with an open cavity design allow for complete release without the use of etch holes scattered across the surface of the mirrors.

The only noticeable flaw in the arrays was the formation of a few small stringers between the same two elements in each of the arrays. After closer examination of the layout, it was found that these two edges were inadvertently spaced only 1.8  $\mu\text{m}$  apart rather than the normal 2  $\mu\text{m}$  used throughout the array. These stringers, shown in Figure 7-22(b), resulted when the edges of the mirrors were snapped to the mask grid as previously described [12]. The resulting “stair-step” pattern joined the surfaces. Activation of either device immediately broke the stringers between the two elements. As evident in Figure 7-22(b), the rounded edges of the remaining elements were clearly defined with no other malformed features.

Although one array completely failed to bond due to planarity issues between the two modules, that array was used to test the behavior of the unbonded actuators. Using the Zygo interferometric microscope, deflection measurements from 20 devices indicated that the actuators behave very uniformly. The maximum variance in peak address potential between devices was found to be roughly 1.6% error.

### 7.4.2 Piston Device Behavior

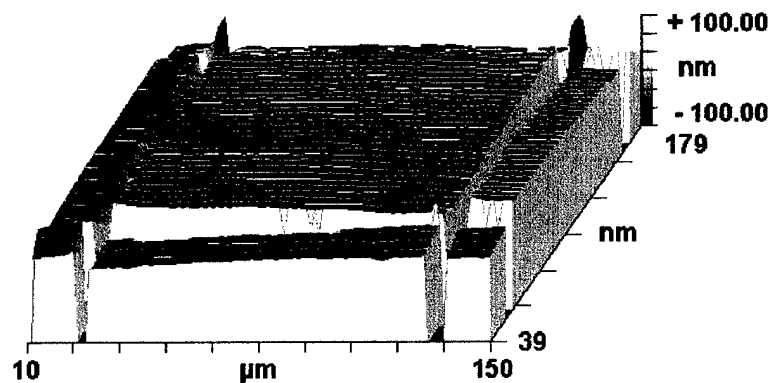
The rectangular piston style micromirror arrays were tested using a Zygo interferometric microscope to determine key features of the array and to characterize each individual micromirror. Figure 7-23 shows typical interferometric intensity patterns induced on a device under test. The uniform lines shown in Figure 7-23(a) demonstrate a very smooth and continuous surface since there are no distortions of the fringing patterns evident anywhere along the surface of the mirror.



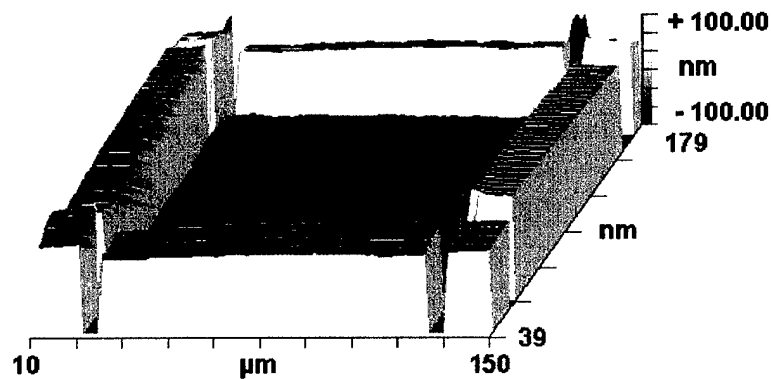
**Figure 7-23.** Photographs of intensity patterns on a rectangular piston device.

The lines shown in Figure 7-23(b), however, illustrate the activation of the central device with a shift in the local intensity pattern. The deflection distance was chosen to maximize the contrast between the resting and activated interferometric intensity maps. The surface deflection shown was the first distance at which the intensity patterns appeared to be perfectly out of phase with the original resting pattern.

The Zygo interferometric microscope sweeps the intensity maps shown in Figure 7-23 across the surface of the array and then calculates the relative deflection of each portion of the array based on the intensity at that position. A three-dimensional image of the resting and activated micromirror device can be generated from this data. Figure 7-24 illustrates the resting and activated positions.



(a) Typical rectangular piston micromirror device in resting position



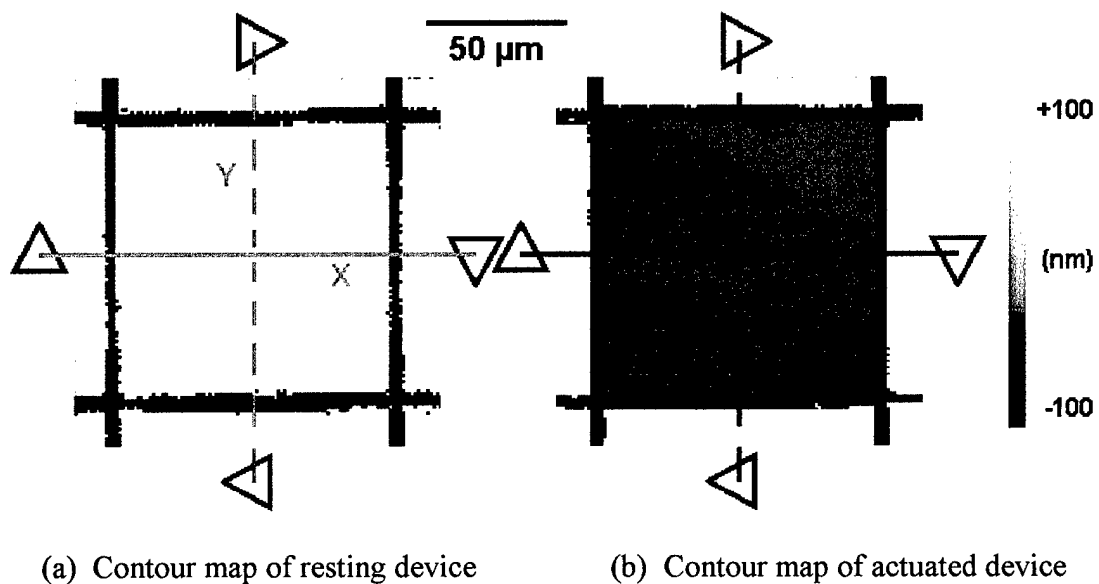
(b) Typical rectangular piston micromirror device in actuated position

**Figure 7-24.** Surface relief maps of a typical piston micromirror device.

The rectangular piston device shown in Figure 7-24 illustrates several key characteristics that are desirable for individually addressable arrays. First, the array

demonstrates nearly ideal planarity. The vertical scale of these plots is highly exaggerated showing 200 nm of variance across the 140  $\mu\text{m}$  square characterization window. The worst case planarity variance across a 1 mm array was measured to be less than 80 nm while the worst case device showed roughly 20 nm of variance across the 100  $\mu\text{m}$  surface for a worst case tilt of only  $0.01^\circ$  from the normal of the array.

A more precise measurement of surface deflection can be obtained using the deflection profile feature of the microscope. Figure 7-25 shows a contour plot of the resting and actuated deflection data across the device under test.

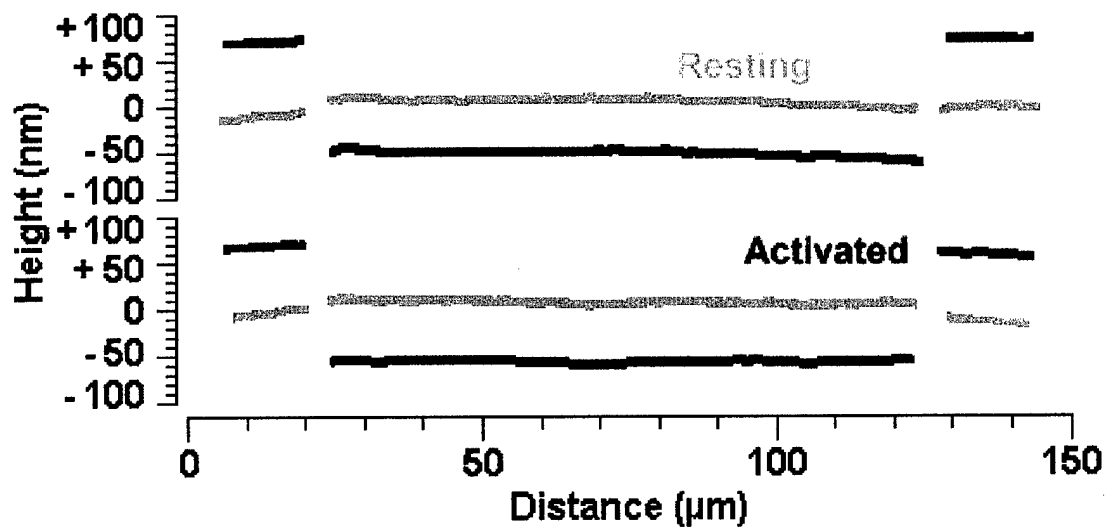


**Figure 7-25.** Surface contour maps of a rectangular piston micromirror device.

These contour maps show no measurable cross-talk between devices. The bonding anchors shown in Figure 7-1 form grounded bonding columns that surround the address electrodes of each device. These supports create a nearly ideal shield through which electrostatic fringing lines cannot interfere with other devices [14].



Using this more quantitative representation, a line can be drawn along any portion of the surface in order to view the profile along the specified path. The contour plots in Figure 7-25 show lines drawn along the  $x$  and  $y$  axes of the micromirror surface including portions of neighboring devices. Figure 7-26 illustrates the resulting deflection data for the device both at rest and while activated.

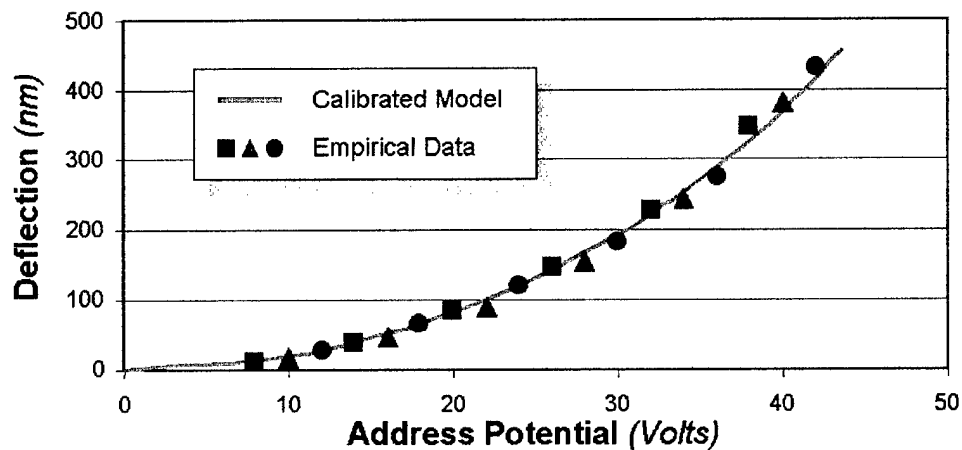


**Figure 7-26.** Plot of deflection profiles for a rectangular piston micromirror device.

Again, the vertical scale is highly exaggerated from which it is apparent that no adverse behavior is observed during the activation of the device. These profiles demonstrate that the device actuates in a nearly ideal piston or “phase-only” manner such that no unwanted tilt is observed in the mirror surface.

As discussed in Chapter 5, a characteristic model of the devices was developed and used to test device performance. Deflection data was averaged using deflection profiles like those shown in Figure 7-26 as a function of applied address potential. A typical deflection versus address potential curve was created for all

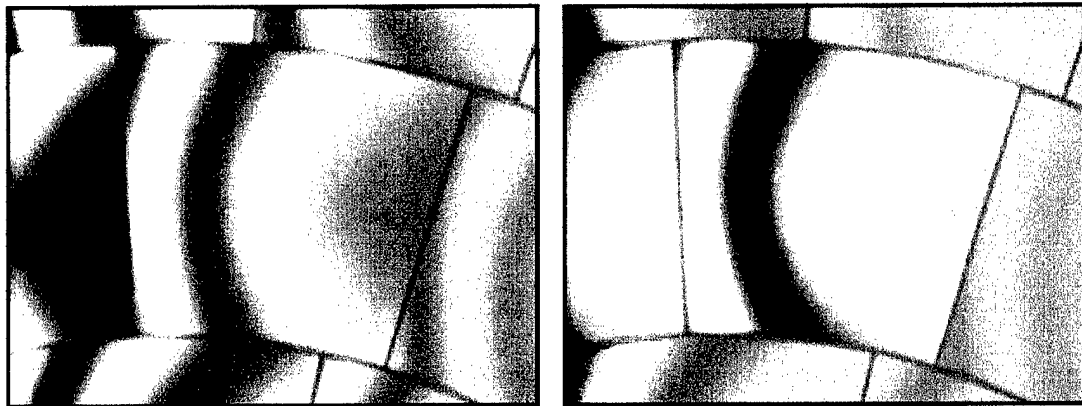
devices using standard electrostatic and deflection force balance techniques [14]. Although the spring constant can be predicted using the geometry and material properties of the support flexures of the device, significant variability in the material properties of MUMPS layers makes it more reliable to simply calibrate the spring constant to empirical data of a piston device. Figure 7-27 shows such a calibrated model along with data measured from typical piston devices.



**Figure 7-27.** Plot of characteristic behavior of a rectangular piston device.

All of the piston style arrays demonstrated consistent behavior and fully activated within 10-15% of predicted address potential. Other devices with lower spring constants and elevated address electrodes deflected to as much as 600 nm when CMOS compatible address potentials were applied. Since the bonding column of the device is placed beneath the mirror surface, the deflection is limited to 750 nm which is the thickness of the oxide layer between them. Devices with the bonding structures and flexures place around the outer edge of the mirror would have roughly 80% active surface area, but could achieve stable deflections of 3  $\mu\text{m}$  or more.

Using the same testing techniques as the rectangular array, the polar piston arrays were characterized for surface uniformity and device deflection. The effect of the large gold bond pad connected to the mirror surface became immediately apparent as the intensity map was induced on the array. As shown in Figure 7-28, the lines along the surface of the devices are slight curved which indicates that the surfaces of the mirrors are not perfectly flat, but slightly warped due to residual stress.



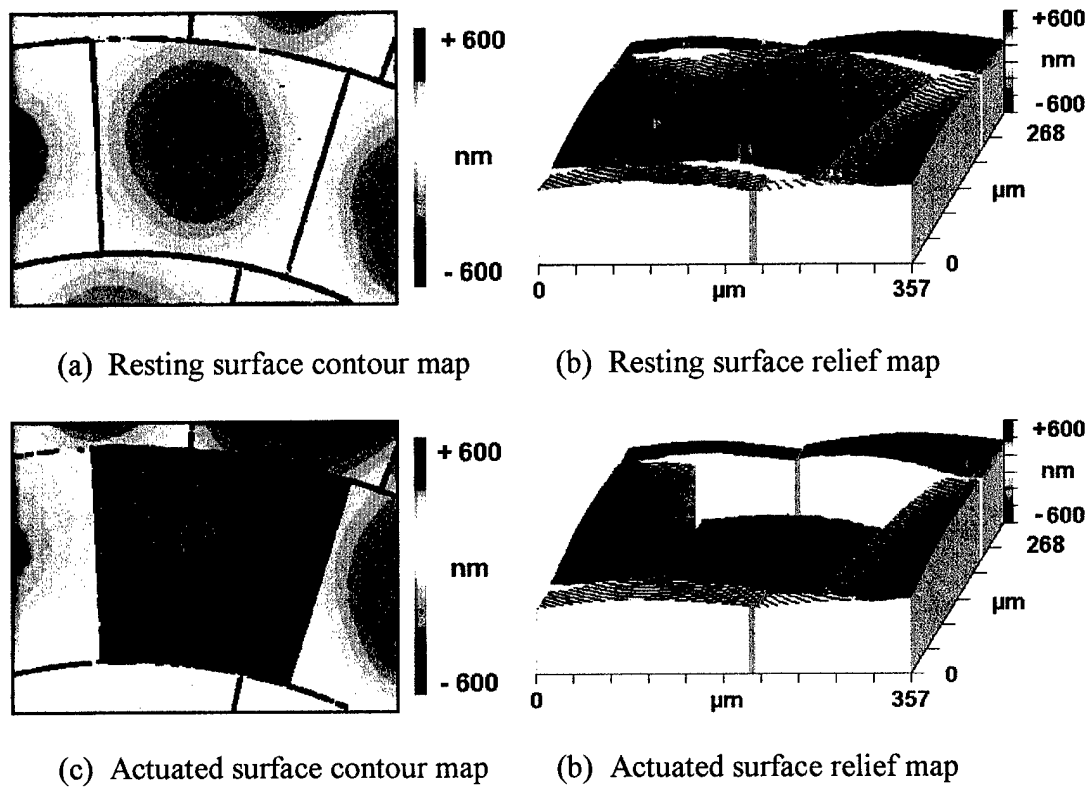
(a) Resting polar piston element

(b) Actuated polar piston element

**Figure 7-28.** Photographs of intensity patterns on a polar piston micromirror device.

Although the surface is slightly curved, the resting position of a typical polar element shown in Figure 7-28(a) indicates that the intensity pattern is generally continuous across several devices such that none is deflected relative to another. The intensity pattern shown in Figure 7-28(b), however, clearly shows segmented lines which indicate that the device is deflecting. From these intensity patterns it is already clear that the mirror surface does not significantly deform during actuation since the general shape of the intensity pattern is preserved between the two positions.

The arrays were characterized for deflection behavior as a function of address potential and to identify any tilting or other adverse operation of the mirror surface. The surface characterizations shown in Figure 7-29(a) and (b) indicate that the resting device under test is relatively parallel to the surrounding devices. Again the vertical scales of these plots are very highly exaggerated to show the surface detail.



**Figure 7-29.** Characterization of a polar element in resting and actuated positions.

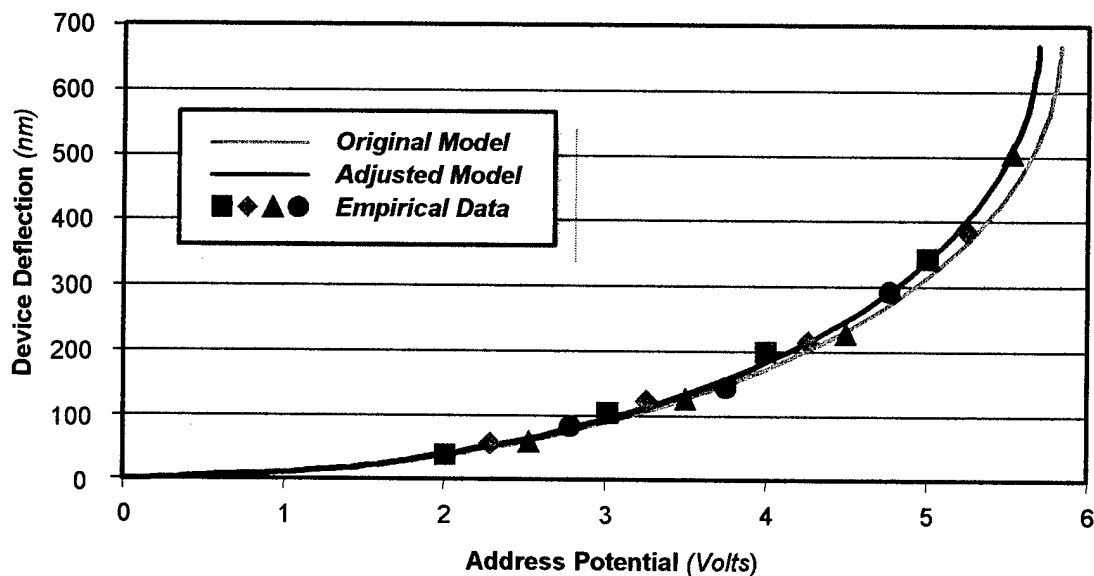
The device is again measured at various address potentials until it finally comes to rest on a safety stop that prevents the upper electrode of the actuator from shorting with the lower electrode. Figure 7-29(c) and (d) show the device at full deflection in which the surface rests approximately 732 nm below the surface of the array.

Just as the intensity pattern in Figure 7-28(b) shows that the central device is positioned along a different plane than the surrounding devices, the contour map in Figure 7-29(c) and the relief map in Figure 7-29(d) show the deflection of the device with a precise characterization of the mirror surface. From these characterizations, several points on the surface of numerous devices were found to deflect uniformly such that no adverse tilt in the mirror surface was observed during operation.

Additionally, characterizations were made on resting devices while actuating adjacent devices to test the effects of cross-talk that can normally be a problem with actuators in close proximity within an array [10]. In all cases, any resulting deflected position was indistinguishable from the resting characterization which indicates that the ground plane surrounding each actuator does indeed diminish adverse electrostatic effects that would normally be noticeable with such large mirror surfaces.

As evident in, the mirrors consistently displayed roughly 100 nm of curved surface variance along the 200  $\mu$ m radial direction resulting in a 200 mm radius of curvature. As previously described, this was a known side effect of the large and robust bond pads used with the mirror surfaces on the host module. Unfortunately, the mirror surface bond pad configuration chosen was probably the worst arrangement to use. Opposite corners of the bond pad induce a stress along lines extending to opposite corners of the mirror surface which are the longest stretches of each element. Rotating the bond pad structure 45° or reducing the four distributed mirror posts to a single post at the center of the element would reduce the curvature. Unfortunately, the residual polysilicon stress of the MUMPS process would likely create some smaller persistent curvature typical of larger surfaces.

The deflection characterization of these devices produced outstanding results. Typically, predicted models for such devices can be adjusted by as much as 10-20% to fit empirical data [4]. With surface-micromachined devices, the drawn flexure dimensions, published layer thickness data, and expected material properties are target values around which true values display some error. Figure 7-30 shows a typical behavior plot of predicted and adjusted models characterizing deflection data versus address potential from four different devices within two different arrays.

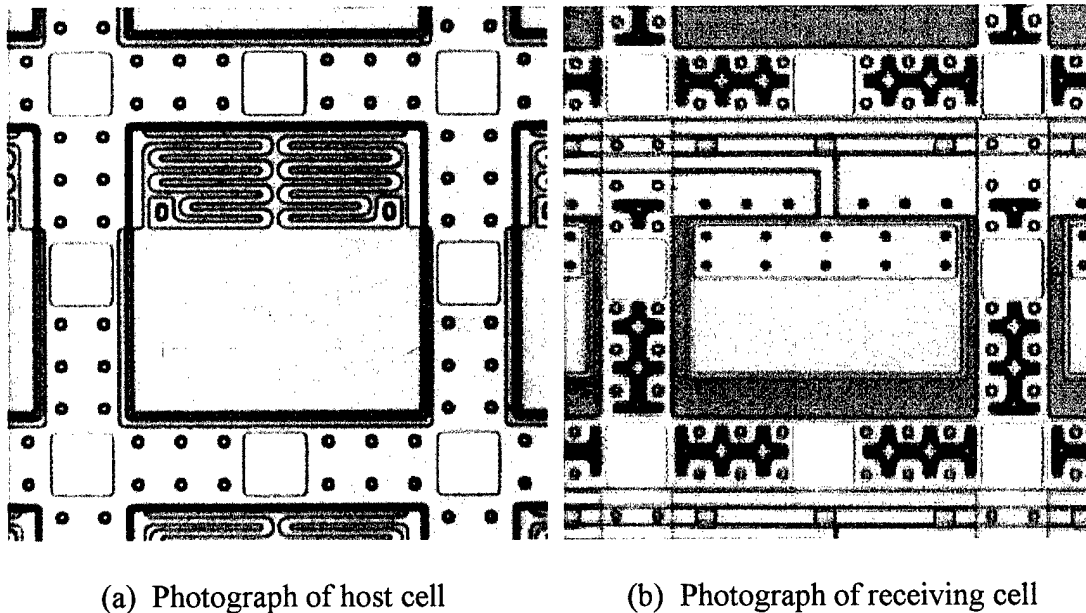


**Figure 7-30.** Plot of characteristic behavior for several polar piston devices.

As observed in Figure 7-30, the predicted model for the standardized polar actuator was remarkably close to the measured deflection data of the polar elements. In fact, the calculated spring constant of 1.0495 N/m using layout dimensions was adjusted to only 1.01 N/m to fit the data to the adjusted model curve. In this case, it is most likely that the right combination of modeling errors simply cancelled out.

#### 7.4.1 Bonding Characteristics of Cantilever Arrays

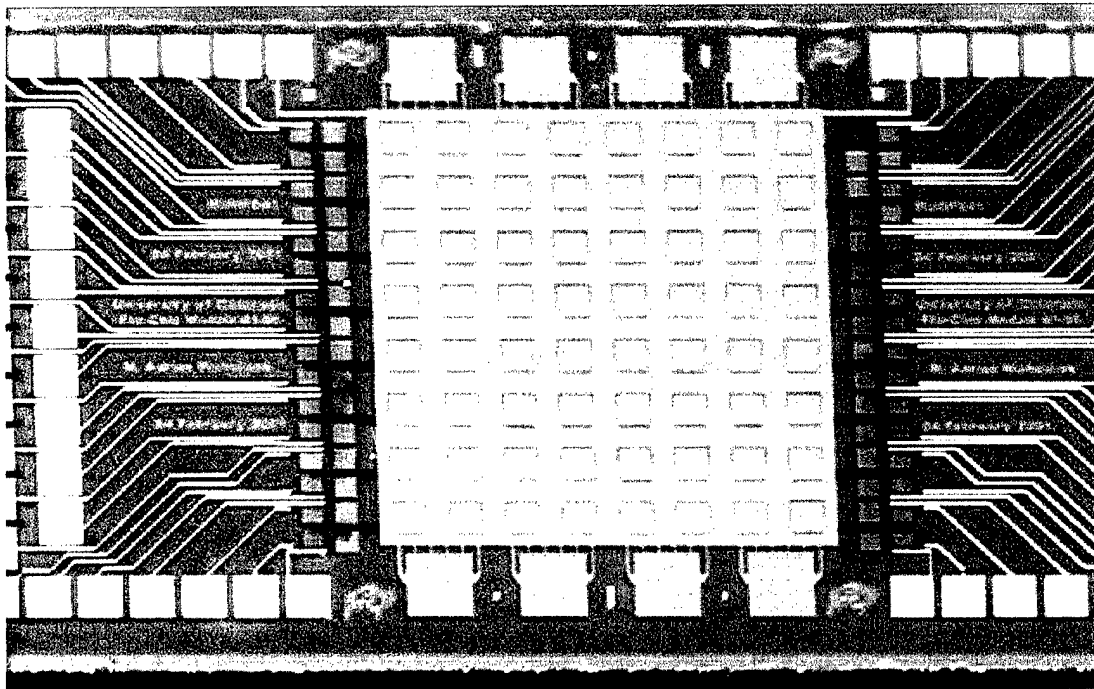
A visual inspection of the cantilever devices shows that the host and receiving cells are properly formed. The rounded flexures shown in Figure 7-31(a) were designed to reduce stress concentrations, but are usually the first to be malformed if any fabrication errors are found. The receiving cell in Figure 7-31(b) shows some erosion of the grounded landing pad due to the previously described galvanic effect.



**Figure 7-31.** Photographs of host and receiving cells of a typical cantilever device.

The discoloration of the landing pad is clearly evident in which the galvanic effect observed during release tends to remove dopants from the thin lower layer of polysilicon connected to large amounts of gold [25]. Although this effect does not prevent the operation of the devices, long address wires consisting of the resulting porous polysilicon can show considerably increased resistivity.

Once these opposing modules are bonded, the arrays are released and dried as previously described. With the exception of the primary failure mechanisms discussed with the process yield analysis, there were few other problems associated with the process. Numerous arrays of cantilever devices were bonded with no measurable alignment errors or adverse behavior in the mirror surfaces. Figure 7-32 shows a photograph of one typical cantilever micromirror array.



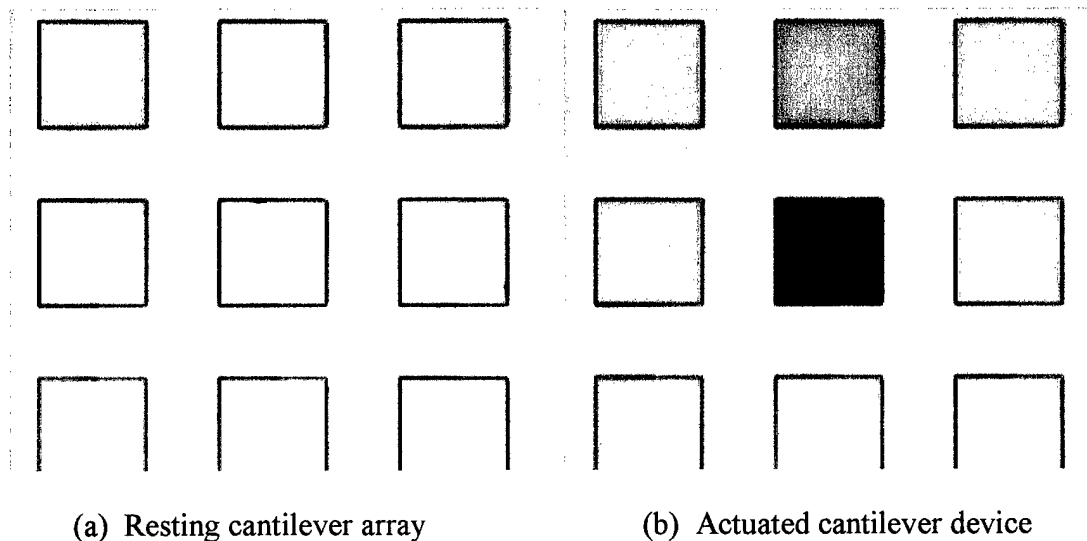
**Figure 7-32.** Photograph of a typical released cantilever flip-chip micromirror array.

Like many others, this array uses eight large bond pads to secure the array and to minimize alignment errors. Although individually bonded devices within arrays with as much as 97.8% active surface area have been created, most arrays use the common frame surrounding each device to simplify the bonding process. Unfortunately, the average yield in producing such flawless arrays is only 30% using this process.



#### 7.4.4 Cantilever Device Behavior

Like the piston flip-chip arrays, the deflection of devices within the cantilever arrays was characterized to determine the success of the assembly process. As previously described, some of the very first cantilever arrays demonstrated adverse characteristics that were specifically identified and removed by designing arrays with a variety of improved features. The behavior of the original cantilever array is shown in Figure 7-33 in which the central device is shown at rest and fully actuated.

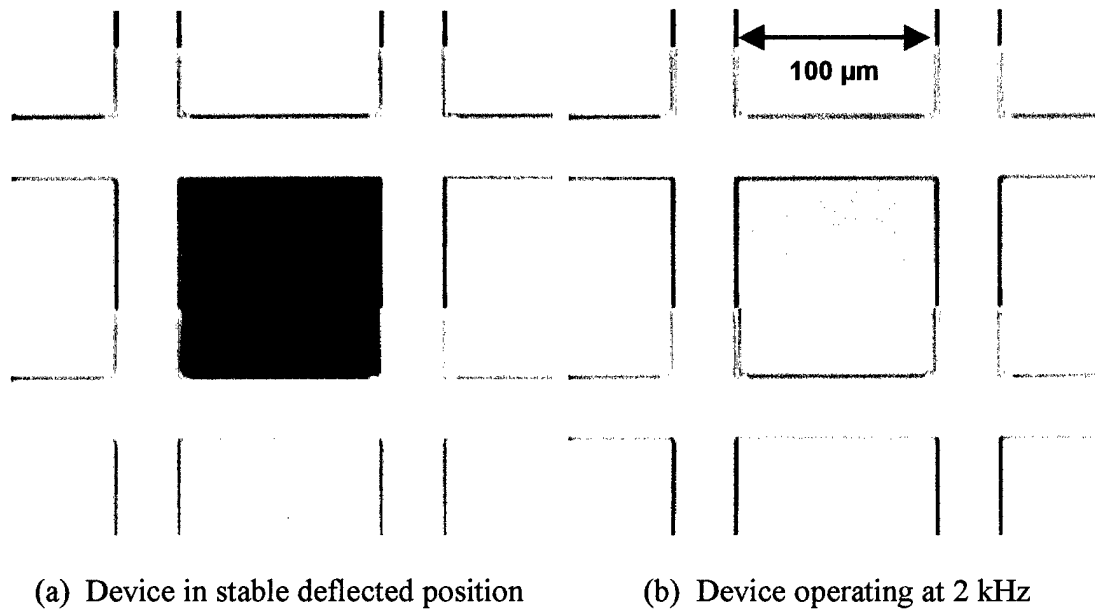


**Figure 7-33.** Photographs of original flip-chip cantilever micromirror operation.

Although the devices achieved desired tilt angles up to a  $15^\circ$  maximum, there were adverse effects observed in first-generation devices. First, these particular devices land on the nitride isolation layer of the receiving module rather than a grounded landing pad. The high address potentials ranging from 64 volts to 98 volts tend to charge the surface and interfere with neighboring devices. Although electrostatic

cross-talk is not an issue for these arrays since the continuous bonding frame between devices are grounded, Figure 7-33(b) clearly shows some unwanted deflection in neighboring devices due to charging of the nitride surface. For this reason, switching times for these particular devices ranged from 200 msec to nearly 800 msec depending on the spring design of the device.

The charging effect was removed by adding an extended polysilicon ground plane throughout all exposed areas of the devices which also acts as a grounded landing pad for the mirror surface. Figure 7-34 shows the operation of an improved array of cantilever devices in which high frequency switching is now possible.



(a) Device in stable deflected position (b) Device operating at 2 kHz

**Figure 7-34.** Photographs of improved flip-chip cantilever micromirror operation.

Like most flip-chip arrays, the mirror surfaces rest approximately 10 μm off the surface of the substrate. If the bonding columns between adjacent devices were formed as continuous walls, the air inside the device would be trapped except for the

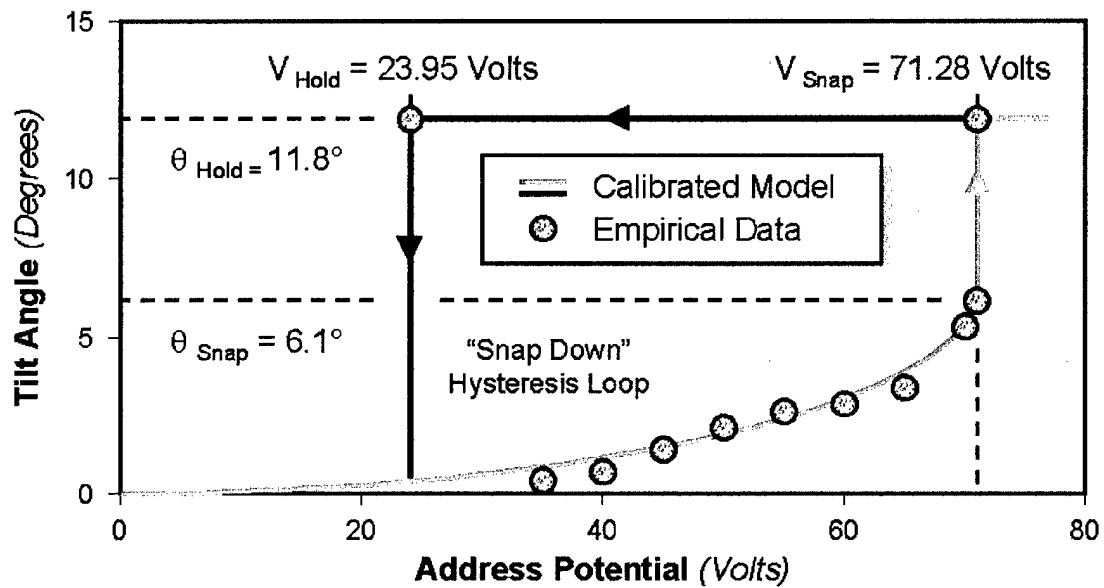
narrow 2  $\mu\text{m}$  gap surrounding the mirror surface. As a result, squeeze film damping would dramatically reduce the switching frequency of such devices as the air rushes in and out of the cavity during operation. To avoid this, the gold pads and via cuts between polysilicon layers are segmented so that the air can pass through each device yet maintain a grounded wall between them to shield against electrostatic cross-talk.

Rather than using an expensive strobe system to validate switching of the device, the refresh rate of a typical probe station camera can be used to count increases in drive frequency. If the drive frequency of the micromirror device was truly synchronized with the sample frequency of the camera, no motion would be visible. However, any slight difference between the two frequencies produces a phase variance inherent to sampling periodic signals at a rate near the drive frequency. As a result, the mirror appears to be switching at a much slower phase or “beat” frequency. As the drive frequency increases through each harmonic of the 60Hz fundamental camera rate, the phase variance cycles more quickly such that the mirror appears to be switching increasingly faster. The result is an effective ladder of quantified steps that can be observed in sequence to validate the motion of the device.

Without very precise adjustments at higher drive frequencies, however, the apparent motion of the device becomes indistinguishable between harmonics. A drive frequency of approximately 1.08 kHz is sufficient to blend the resting and activated samples of the mirror motion into a single continuous image. In order to continue to characterize the mirror using this technique, the true fundamental sample rate of the camera must be known with much greater precision to reduce the effective phase frequency relative to the mirror.

Rather than scan each step for the actual frequency, it was observed that the continuous image of the moving mirror became noticeably irregular and noisy at the precise point in which the increasing drive frequency swept through the actual synchronized harmonic. As a result, the true switching frequency of the mirror surface could still be validated without closely observing the apparent phase motion of the device. Continuing with this second technique, the drive frequency was stepped through 2.10 kHz beyond which no further characteristics were observed.

Using the interferometric microscope, the rotation of a typical mirror surface was measured as a function of applied address potential. Figure 7-35 shows a behavior curve and empirical data for a typical cantilever micromirror device.



**Figure 7-35.** Plot of angle versus address potential for a flip-chip cantilever device.

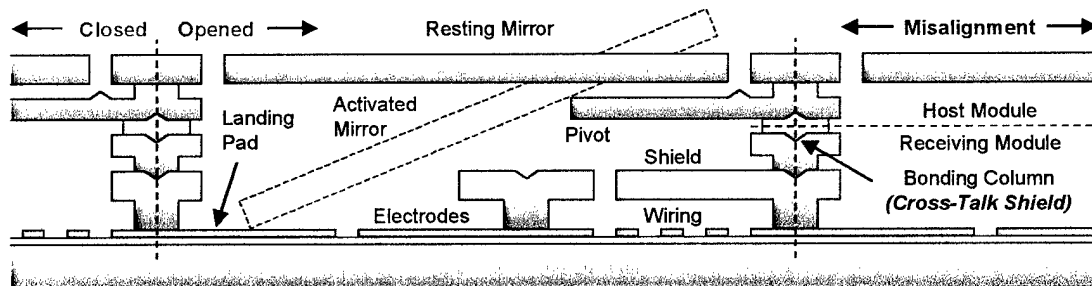
As previously described, the electrostatic capture of such a device produces a hysteresis loop that is observed once the device snaps down. The curve was

calibrated to the resting angle and to the angle and address potential at which the device snaps down to the receiving substrate.

One distinct characteristic of the device behavior is the variance about the ideal model prior to snapping down. Depending on the type of flexure used to support the device, the mirror surface will exhibit piston operation at lower voltages and may resist tilting until contact is made with the pivot upon which the mirror rests once snapped down. Some mirrors then exhibit further resistance to tilting and require a higher address potential to continue rotating beyond the pivot. Furthermore, the pivot tends to interfere with the motion of the mirror surface as it deflects such that deflection data varies between tests. The data in Figure 7-35 illustrate this behavior showing that the true angle varies slightly from the model in the region where the mirror surface is in contact with the pivot.

As originally illustrated in Figure 7-1(d), the mirror surface is in very close proximity to the address electrodes after it snaps down. Since the electrostatic force is inversely proportional to the height of the gap, the address potential required to snap the mirror down,  $V_{\text{Snap}}$ , is much greater than the potential required to hold the mirror,  $V_{\text{Hold}}$ , in the deflected position. These values are shown in Figure 7-35 along with the angle of the mirror just prior to snapping down,  $\theta_{\text{Snap}}$ , and the stable deflected angle,  $\theta_{\text{Hold}}$ , where the mirror rests against the pivot and the landing pad. This device achieved  $11.8^\circ$  of tilt which was less than the target angle of  $12^\circ$  when designing the layout of the device. The most likely causes of this slight error are the compression of the gold layers during bonding and a variation in the actual thickness of each layer from the published thickness of the MUMPS process.

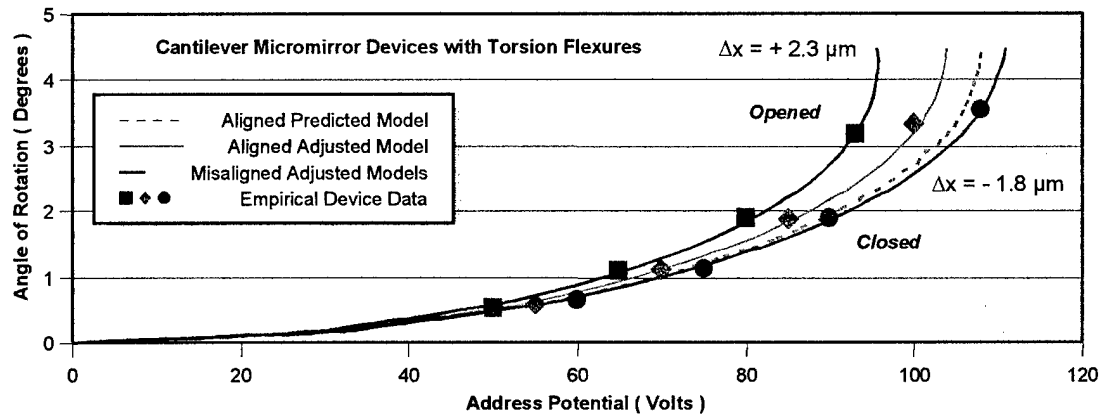
Because the size of each mirror surface is designed to be slightly smaller than the window of the receiving cell upon which it is bonded, typical devices can tolerate at least 4  $\mu\text{m}$  of lateral alignment error. Although these devices could be made to tolerate much greater errors, most are optimized for address potential or other characteristics that force a trade-off with alignment tolerance. Specifically for cantilever devices, an alignment error along the direction of motion can create a very noticeable difference in the address potential required to actuate the devices. For instance, the mirror surfaces shown in Figure 7-36 can either be bonded to the left or right of the ideal position. In doing so, the lateral distance between the electrodes and the axis of rotation will be closed and opened, respectively.



**Figure 7-36.** Illustration of direction of alignment error for cantilever devices.

As discussed in Chapter 5, the centroid position at which the electrostatic force from the electrodes is applied determines the magnitude of the electrostatic torque that actuates the mirror surface. Since the worst case alignment variance of 4  $\mu\text{m}$  between the two extremes is possible, such alignment errors would produce very different behavior curves for those devices. Unfortunately, a wide range of device behavior was indeed observed since performance is so sensitive to array alignment.

To predict the behavior of a typical cantilever device with a torsion flexure, the predicted model of an ideally aligned device can be found using the layout dimensions and published thickness and material properties of the flexure layer. The torsion spring constant was determined to be  $3207.35 \mu\text{N}\cdot\mu\text{m}$  for one such device. The plot in Figure 7-37 shows the original aligned predicted model.



**Figure 7-37.** Plot of characteristic models for several torsion micromirror devices.

The adjusted constant of  $2965 \mu\text{N}\cdot\mu\text{m}$  was found by fitting the curve to the average measured rotation of several devices within an array that was near perfectly aligned. The rotation data for one of these devices is shown along the aligned adjusted model.

The effect of an alignment error can be seen in the characterization data for two identical torsion flexure arrays that were each bonded with an approximate alignment error of  $2 \mu\text{m}$  in opposite directions. The first was bonded such that the torsion flexure was placed nearer to the electrodes than ideally positioned. The distance between them was thereby closed such that the centroid position and therefore the electrostatic torque was somewhat reduced. Conversely, another array

was bonded such that the torsion flexure was placed further from the electrodes. The distance between them was opened such that the centroid and electrostatic torque were somewhat increased. The net effect of this alignment error on the behavior of each device is simply to increase and decrease the address potential, respectively, that is required to deflect the mirror surfaces to a desired angle.

To account for the alignment error, the position of each model was adjusted to fit the data of the misaligned devices. Using the adjusted spring constant, the misaligned models were calibrated using a position correction of  $-1.8\text{ }\mu\text{m}$  for the closed device and  $2.3\text{ }\mu\text{m}$  for the opened device. These models are also shown in Figure 7-37 along with measured rotation data.

It should be noted that devices with serpentine flexures were not designed for continuous operation and were therefore not compared to this model. These binary style devices were designed to rest on a pivot such that the mechanical contact prevents any smooth and regular rotation of the mirror surface. Additionally, several styles of torsion devices were created using the same design features of the cantilever devices. The torsion devices tilt in two directions exactly as the cantilever devices tilt along a single direction. The address electrode, bonding assembly, and flexure configuration are simply mirrored along the central axis of the device such that the model applies in either rotation direction. Not surprisingly, the torsion devices demonstrated almost exactly the same alignment errors and corresponding device performance as the cantilever arrays.



## 7.5 Conclusions

This chapter presents the design, commercial prefabrication, assembly and testing of advanced micromirror arrays fabricated using a novel, simple and inexpensive flip-chip assembly technique. Several piston, cantilever and torsion micromirror arrays were fabricated using flip-chip assembly by which the upper layers of the array are fabricated on a separate chip and then transferred to a receiving module containing the lower layers. Typical polar piston arrays boast 98.3% active surface area, highly planarized surfaces, low address potentials compatible with CMOS electronics, highly standardized actuation between devices, and complex segmentation of mirror surfaces which allows for custom aberration configurations. Continuous torsion devices offer stable operation through as much as six degrees of rotation while binary cantilever devices offer stable activated positions with as much as 20 degrees of rotation. All arrays have desirable features of costly fabrication services like five structural layers and planarized mirror surfaces, but are prefabricated in the less costly MUMPs process. In short, the flip-chip assembly process enables fast, reliable, simple and repeatable fabrication of advanced micromirror arrays at a much lower cost than other foundry services.

A process yield analysis shows that the bonding and release etch steps of the flip-chip fabrication process are the most common sources of damage to flip-chip modules for a variety of reasons. Although the bonding yield has steadily improved with the advent of better design and bonding machine calibration techniques, the release process remains the critical portion of the process. This phase of the flip-chip assembly process is by far the most destructive of the entire fabrication method and

requires specific techniques and considerations to reduce damage to the flip-chip modules. Many of the observed failure mechanisms have already been overcome with the modification of release procedures or by improved design of micromirror host cells. Others, however, remain a source of concern and must be carefully studied before the flip-chip fabrication process can progress to large production volume. Ultimately, the flip-chip fabrication process remains a viable means to create low-cost prototypes of advanced micromirror arrays.

## CHAPTER 8

### FLIP-CHIP ASSEMBLY ONTO CMOS ELECTRONICS

This chapter presents the design, fabrication, and testing of various arrays of cantilever micromirror devices integrated atop CMOS control electronics. After MUMPs prefabrication, the upper layers of the arrays are flip-chip transferred to CMOS receiving modules using a novel latching off-chip hinge mechanism presented in the following chapter. This mechanism allows the micromirror arrays to be released, rotated off the edge of the host module and then bonded to the receiving module using a standard probe station. The hinge mechanism supports the arrays by tethers that are severed to free the arrays once bonded. The resulting devices are inherently planarized since the bottom of the first releasable MUMPs layer becomes the surface of the integrated mirror. The working devices are formed by mirror surfaces bonded to address electrodes fabricated above static memory cells on the CMOS module. These arrays demonstrate highly desirable features such as compatible address potentials, less than 2 nm of RMS roughness, approximately 1  $\mu\text{m}$  of lateral position accuracy and the unique ability to metallize reflective surfaces without masking. Ultimately, the off-chip hinge mechanism enables very low-cost, simple, reliable, repeatable and accurate assembly of integrated microsystems without specialized equipment or complex procedures.

## 8.1 Introduction

One of the most valuable developments in MEMS is the ability to integrate surface-micromachined devices with control electronics. It has been very difficult to fabricate both on the same chip due to the temperature and sacrificial layer incompatibility between them. Therefore, less ideal means of integration have been used. First, the use of Multi-Chip Modules (MCMs) has been widely employed to connect the input and output devices of electronics chips to those of MEMS chips. Second, the flip-chip bonding of CMOS electronics onto MEMS substrates is a well known technique used to minimize wiring traces and increase wiring density. Finally, simple MEMS structures can be prefabricated beneath the surface of a wafer intended for CMOS processing using the Integrated MEMS (IMEMS) “trench prefabrication” technique developed by Sandia National Laboratories [7]. These techniques, however, are only a wiring improvement between components and do not increase the performance of MEMS structures nor enable new devices. Such integration simply does not achieve the level required by many demanding applications.

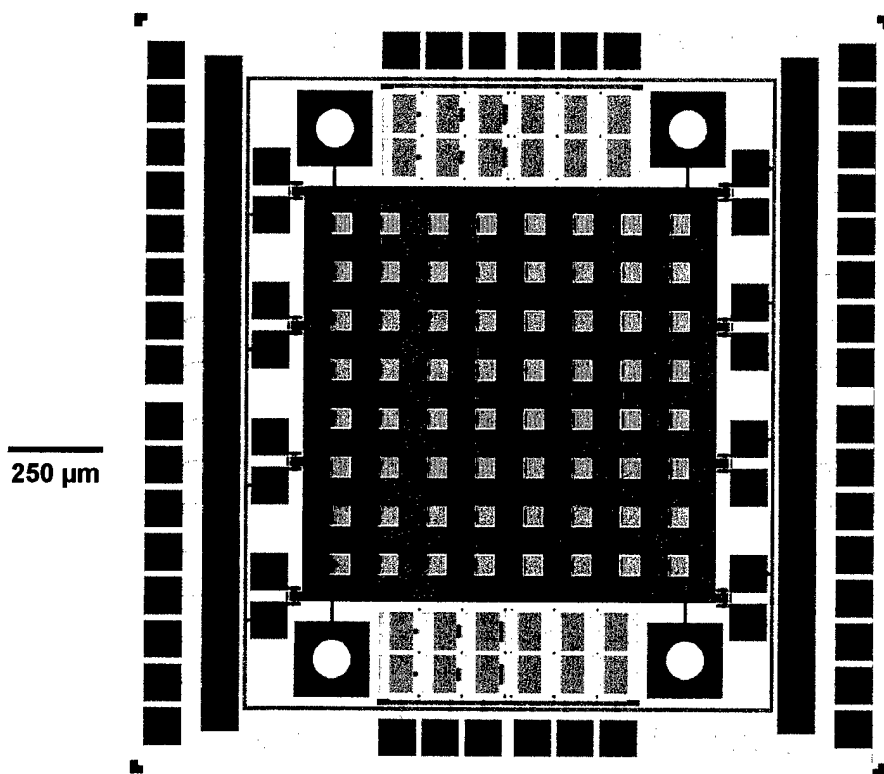
Unlike these standard techniques, flip-chip assembly allows improved MEMS performance by directly coupling mechanical devices to electronics. For instance, an array of electrostatically actuated micromirrors must have at least two layers to form the upper and lower electrodes of the device. Additionally, addressing each device within large arrays may require numerous layers to achieve the necessary wiring density. On the other hand, if that array could be flip-chip bonded atop an opposing array of latching cells on a CMOS chip, the combined layers and static memory of the two chips would form a far more advanced microsystem. Individual MEMS devices

can be activated and latched into position with the control electronics integrated on the same chip where the micromirror devices are mounted directly over the CMOS address cells. In this manner, the performance of a typical device is drastically improved, especially since the CMOS oxide layers inherently prevent shorting of collapsed devices. This ability to truly integrate MEMS and CMOS is one of the most promising benefits of flip-chip assembly.

### **8.1.1 Background**

Although a wide variety of micromirror arrays have already been fabricated using flip-chip assembly methods, the integration of these arrays atop CMOS modules prevents their release after bonding. The same etch that frees the host substrate and releases the flip-chip components would also remove the oxide layers within the CMOS components and thereby render them useless. One solution would be to use an alternate surface-micromachining process in which a different sacrificial material could be selectively etched without damaging the CMOS layers. Unfortunately, finding suitable materials to perform this task is difficult. Most importantly, however, the cost of doing so may exceed the benefit of the intended microsystem. One of the desirable features of integrating MEMS and CMOS using flip-chip assembly is that the standard commercial prefabrication services are relatively fast and inexpensive. Therefore, in order to maintain the advantages that are uniquely enabled by flip-chip assembly, the process must simply be modified to protect the CMOS receiving modules.

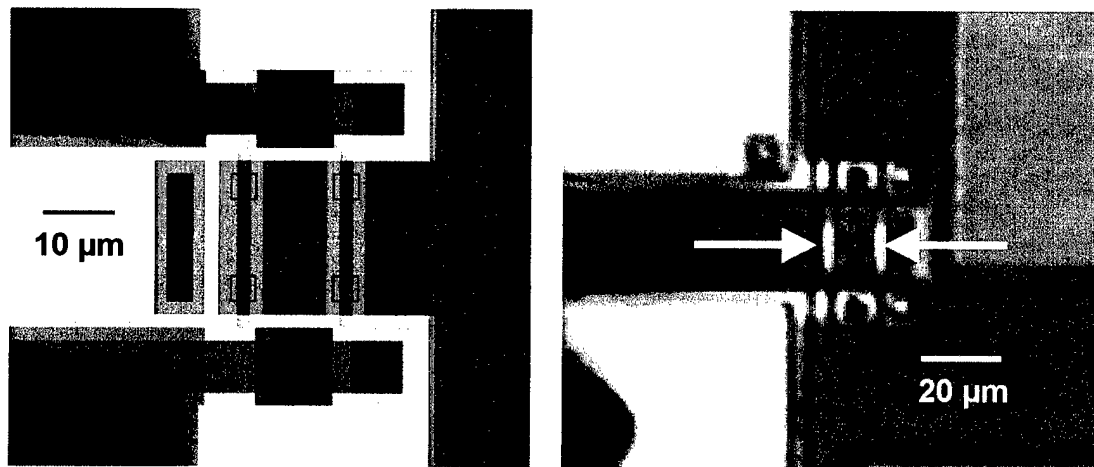
To adapt the flip-chip process for use with CMOS receiving modules, the technique is slightly altered to allow for the release of micromirror arrays before integration so that the CMOS layers are never exposed to any chemical etch. Several arrays were loosely anchored to the host substrate by tethers, fuses or latches that are designed to be broken, burned and opened, respectively. For instance, the array shown in Figure 8-1 uses eight locking fuse mechanisms to hold the array in place.



**Figure 8-1.** Layout of flip-chip micromirror array showing fuse mechanism anchors.

Except for the addition of the locking fuse mechanisms surrounding the common bonding frame, this flip-chip array is very similar to previous arrays in the design of individual micromirror devices and the bond pads that anchor the array.

After several different methods of securing arrays for a prerelease etch were investigated with various degrees of success, the most successful technique was determined to be the fuse mechanism. The very first CMOS integration micromirror array shown in Figure 8-1 demonstrated that such arrays could be effectively stabilized after release. Figure 8-2 shows a close view of the fuses which trap the array in all directions with no more than 2  $\mu\text{m}$  of lateral motion.



(a) Close view of fuse mechanism layout      (b) Photograph of glowing fuses

**Figure 8-2.** Illustration of early CMOS integration micromirror array locking fuse.

These features allowed the micromirror arrays to be prereleased without floating off the host module. Ideally, the arrays are ready for bonding using the same flip-chip bonding machine once the fuses shown in Figure 8-2(b) are burned to free the array.

If the host module is placed on the stage rather than the horn, the release mechanisms can be used either immediately before or after bonding to free the host substrate. For instance, a common wiring bus is used to connect all the probe pads of the fuse mechanisms in order to reduce the release of the array to only two address

lines. If any two pads are connected to opposing pads on the CMOS receiving module, burning the fuses to release the array can be done with probe pads located on the CMOS chip after the two modules are bonded. In other words, the modules can be bonded using the standard bonding process and then separated by applying a potential to the CMOS chip. Since the fuses typically burn at 4.2 volts of applied potential, the fuses could be bonded directly to the voltage supply lines of the CMOS chip so that the host substrate is freed from the receiving substrate when the electronics are first powered up for testing.

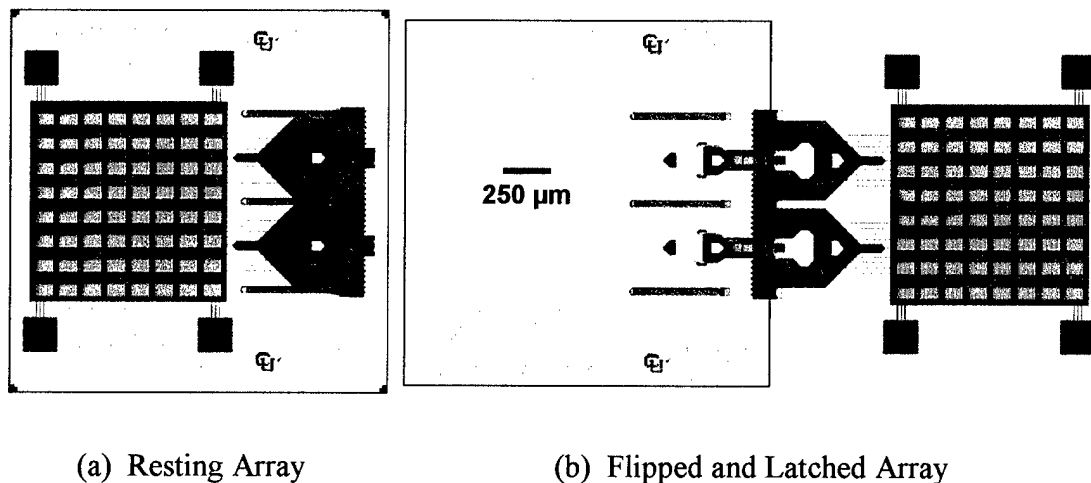
Although the technique of bonding prereleased arrays is capable of producing integrated arrays, the bonding of host structures onto the receiving modules becomes more difficult since they are no longer encased in oxide. This approach routinely demonstrated critical difficulties with two of the most used bonding techniques. First, if solder or adhesive materials are applied to the CMOS receiving module to secure the array during bonding, the materials typically spread out and around the released bond pads on the host module such that the array either bonds to the host substrate or becomes contaminated. In many cases, the arrays were destroyed when half of the array bonded to the host module and the other half bonded to the receiving module.

The other technique involves direct bonding of the metal layers of the two modules at elevated temperatures. Without the use of adhesive materials, slightly higher forces are necessary to facilitate bonding. Unfortunately, the bond pads and the common bonding frame surrounding each device either fractured or shifted such that the final integrated array was not usable. Ultimately, other means of integration would be necessary to avoid these bonding failure mechanisms.



### 8.1.2 Process Overview

The flip-chip assembly technique that has routinely demonstrated the most success is the use of a latching off-chip hinge mechanism that still enables the prerelease of MEMS components, but does not require the flip-chip bonding machine. Figure 8-3 illustrates the use of this mechanism where the flip-chip array is rotated and latched off the edge of the module.



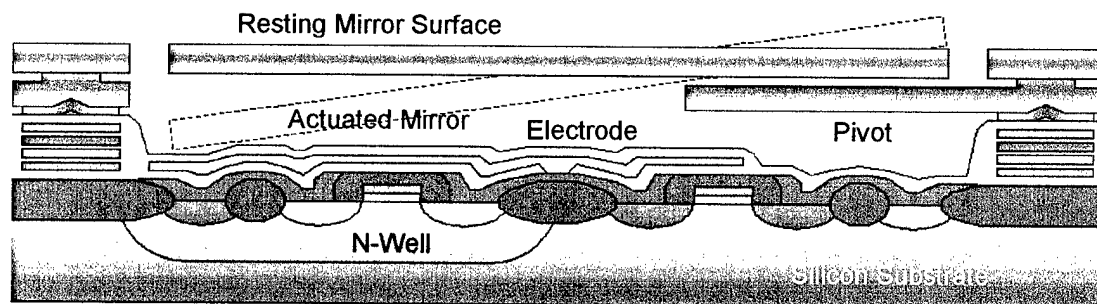
**Figure 8-3.** Illustration of more effective CMOS integration micromirror array.

As shown in Figure 8-3(a), the flip-chip host modules are designed with an 8x8 array of cantilever devices connected to the latching off-chip hinge mechanism which is formed using only the upper two layers of the MUMPs process. Each feature within the mechanism is carefully designed with specific topographical considerations such that all mating elements align properly when rotated and no object interferes with the motion of any other. The micromirror array is attached to the hinge mechanism by tethers that can be severed once the array is bonded. After release, the array is rotated



Although the hinge mechanism was originally designed to reduce alignment error in the flip-chip bonding of variable capacitors on ceramics substrates for a variety of RF applications, it was later found to be very well suited to this form of integration on CMOS electronics. This feature, along with other related bonding techniques, is discussed in much greater detail in the following chapter.

The final integrated arrays will consist of surface-micromachined mirror surfaces that are bonded directly above address electrodes fabricated over latching CMOS address circuits. Each mirror surface is supported by compliant flexures connected to a bonding frame that surrounds it. This frame also provides uniform resting support throughout the array. Figure 8-5 illustrates such a device in which the mirror surface deflects when the CMOS address cell is activated.



**Figure 8-5.** Side view of integrated micromirror bonded to CMOS receiving module.

For this illustration, the address electrode is shown wired to the drain of some arbitrary complementary logic structure. The electrode is formed in the upper metal layer of the CMOS process and remains covered with a thin layer of oxide for isolation from the mirror surface. Although the deflected surface is shown to rest on an active area of the underlying circuit, it should be noted that those areas are sparsely

distributed along the edge of the address cell. As a result, the mirror surface will actually come to rest on an area of field oxide over which the upper layers have been deposited. In short, without the spacer layers shown under each column of the bonding frame, some mirror surfaces would achieve no more than  $2^\circ$  of tilt. The spacer layers elevate the mirror enough for some devices to achieve roughly  $5^\circ$  of tilt.

### **8.1.3 Applications**

Although the ability to effectively integrate MEMS atop CMOS electronics has only recently been developed, the desired applications that have driven the design of such integration are too numerous to count. Virtually any conventional sensor or mechanical device that requires electronic control could benefit from miniaturization using flip-chip bonding. Although not completed within the scope of this research, several integrated systems spanning numerous potential applications were designed to further demonstrate the ability of this flip-chip bonding technique beyond the micromirror arrays presented in this chapter. Among these systems are a variety of MEMS latches, microrelays, reconfigurable antennas, optical switches, and numerous miniaturized sensors that offer improved performance over conventional systems.

For instance, a thin band of polysilicon could be bonded atop a CMOS chip in order to produce an integrated Hall effect magnetometer. Since the sensitivity of this type of sensor increases as the thickness and conductivity of the conductor decrease, such a device offers the potential to realize ultrasensitive magnetometers that are also highly miniaturized and inexpensive to fabricate [16]. Numerous other sensors would also benefit from this type of integration.

#### 8.1.4 Advantages

Similar to the flip-chip assembly techniques presented in other chapters, the integration of MEMS atop CMOS electronics produces highly planarized structures. Additionally, the flip-chip assembly process can be repeated using a single receiving chip to increase the number of structural layers available for an integrated system. Flip-chip integration shares most of the benefits of the standard process, but does not require specialized equipment like the flip-chip bonding machine. All of the flip-chip integration presented in this chapter was completed on a standard probe station.

One of the primary advantages of the flip-chip process is the use of existing commercial services for the prefabrication of both the MEMS and CMOS modules. Since flip-chip assembly is purely a post-process technique, advanced MEMS and integrated microsystems can be created at very low cost. The MEMS modules are prefabricated in the MUMPs process where each of the 1 cm square chips is diced into 2 mm square flip-chip modules. Likewise, a number of commercial CMOS foundries exists which can quickly fabricate receiving chips. The MOSIS service allows easy access to most of these fabrication services through one contact.

Another benefit of this type of flip-chip integration is that the total number of control lines required by an array of devices is dramatically reduced. With a flip-chip array, only the CMOS electronics need be addressed and can be reduced to a simple row/column architecture enabled by CMOS components rather than individually wiring and addressing each device within the array. Therefore, what may have required hundreds of address lines and dual packaging with complicated interconnects now consists only of a single chip with only a few input and output connections.

### **8.1.5 Disadvantages**

Among the disadvantages of the flip-chip integration process is the need for specialized features such as the latching off-chip hinge mechanism. Although very little surface area of the host module is required for many of these features, the process could not be completed without them. Even the simplest flip-chip bonding process still requires the latching off-chip hinge mechanism to position the micromirror arrays over the CMOS receiving modules.

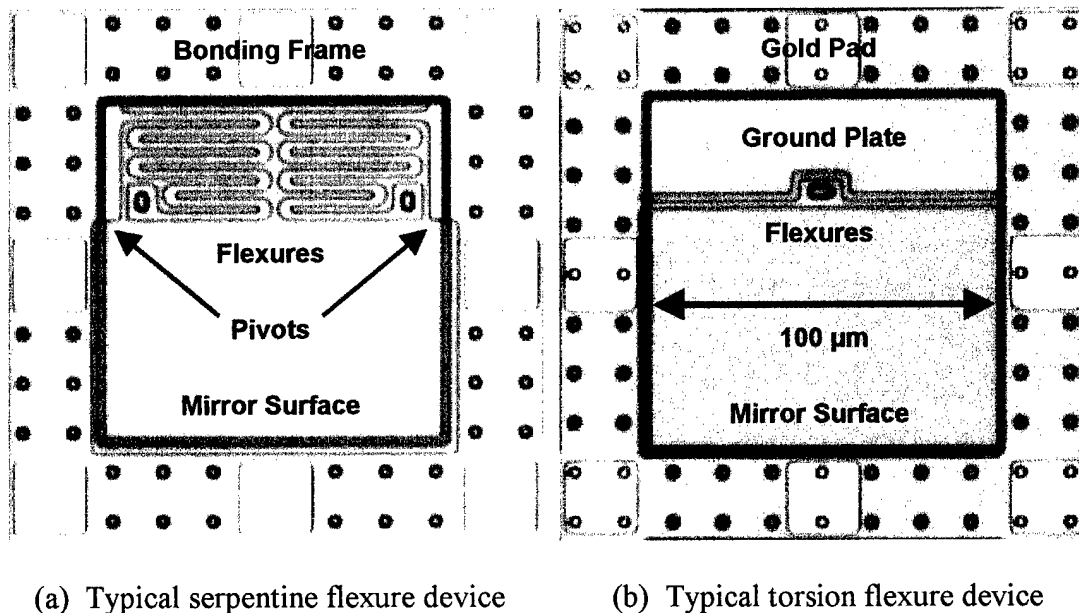
Another disadvantage of this process is the need for some additional and somewhat specialized steps in the fabrication of integrated systems. For instance, a small amount of conductive epoxy must be placed on the receiving module in order to bond the host micromirror array. Although this can easily be done using a probe station or even by hand, the prerelease of the micromirror arrays does not allow the use of the standard thermocompressive bonding. Additionally, the modified release etch itself and the rotation of structures off the edge of the module are steps not shared by any other flip-chip bonding technique. This task requires some practice in order to gain proficiency in effectively lifting and latching structures off the module.

## **8.2 Implementation**

Similar to other flip-chip assembly techniques, the opposing modules are designed and prefabricated independently and then assembled using the techniques specific to CMOS integration. This section describes the design of the host and receiving modules and the assembly of MEMS structures atop CMOS electronics.

### 8.2.1 Design of MEMS Host Modules

The micromirror host arrays designed for CMOS integration are subject to a number of design considerations that are far more demanding than devices fabricated using standard flip-chip assembly. For some devices, the maximum tilt angle is determined by the limit of the drive voltage. Devices already near the limit were designed to rest atop address cells without spacer layers since the added height would further increase the address potential. Additionally, much smaller gold pads were used as spacers around each device to reduce warping of the frame from thermal mismatch stress. Figure 8-6 shows two typical cantilever micromirror devices.



**Figure 8-6.** Examples of two types of typical CMOS integration cantilever devices.

The device in Figure 8-6(a) uses serpentine flexures to reduce address potential, but these flexures are then subject to electrostatic forces in the opposite

direction of the desired rotation. This device requires pivots to help support the deflected mirror surface so that it doesn't simply collapse and rest on the CMOS address cell. The flexures are connected to the mirror surface near the edge of the pivots to reduce the torque that counters the actuation of the device.

The device in Figure 8-6(b) uses pure torsion flexures to produce more ideal motion of the mirror surface. Without the ground plate, these devices are also subject to counter electrostatic forces during actuation and therefore may not fully deflect within the address potential limits of the CMOS process.

Both of the devices in Figure 8-6 are designed to rest atop a large address electrode fabricated in the upper metal layer of the CMOS process. Each device is designed to use the electrostatic counterforces produced by this electrode to help secure the array on the CMOS substrate. The large ground plate and the total area of the serpentine flexures act as an upper address plate and therefore supply a downward force on the bonding frame surrounding each device. As a result, the entire array can be stabilized when only a few devices are actuated. All devices must be carefully modeled to ensure proper actuation at a suitable address potential. Ultimately, all the design features of the micromirror devices are influenced directly by the drive voltage limit of the CMOS fabrication process.

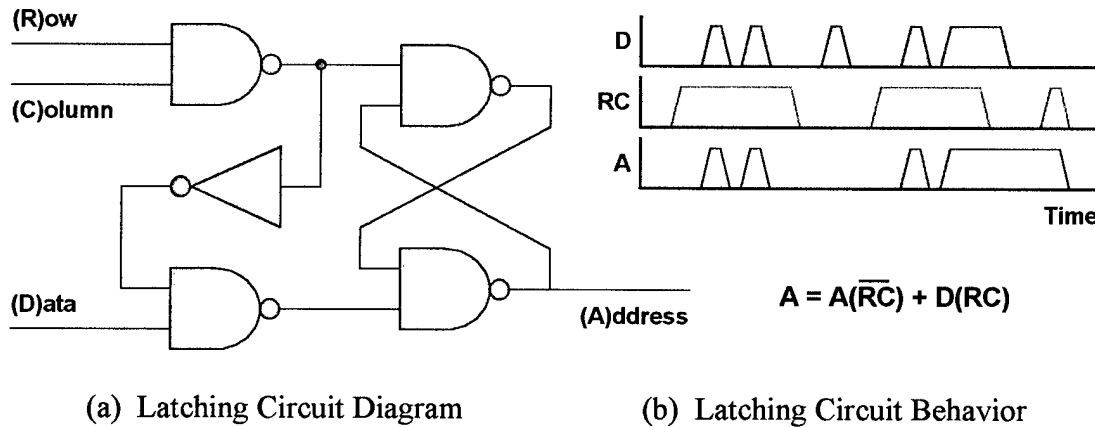
As illustrated in Figure 8-3, the micromirror arrays are connected to the latching off-chip hinge mechanism by tethers that are designed to be broken or burned once the array is in place. Once a standard mechanism is designed, a variety of arrays can be designed and fabricated using the same technique. This off-chip hinge mechanism is described in much greater detail in the following chapter.



### 8.2.2 Design of CMOS Receiving Modules

The CMOS modules presented in this chapter are prefabricated in the American Microsystems, Inc. (AMI) Semiconductor 1.5  $\mu\text{m}$  ABN process which allows upper polysilicon gate structures for increased potential [28]. This n-well process was chosen specifically to facilitate the higher drive voltage, level-shifting circuits, and the additional spacer and metal layers required for the address cells.

The primary portion of the receiving CMOS module is the individual latching cell and address electrode on which each micromirror rests once bonded. Figure 8-7 shows circuit diagrams representing the form and behavior of each cell.

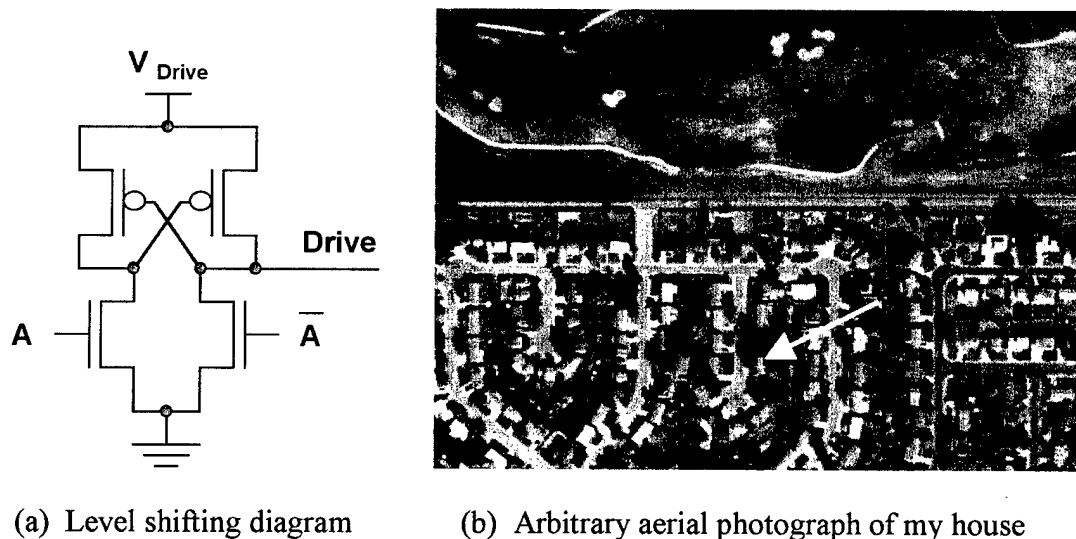


**Figure 8-7.** Symbolic configuration and behavior of each latching circuit.

The symbolic diagram of the latching cell shows a typical data latch that is slightly modified to incorporate both row and column signals to enable the cell. This circuit allows the device to be switched by the data,  $D$ , line as long as the device is active where the row,  $R$ , and column,  $C$ , lines are high. The trace behavior illustrates that the micromirror device can be toggled between resting and activated positions while

the row and column signal,  $RC$ , is active. This will allow the testing of individual devices for frequency response and cross-talk within the array. Once the row and column signal is removed, the value of the data line is latched into the feedback loop of the circuit and the cell address signal,  $A$ , is maintained until it is reset by once again activating the cell.

One of the largest barriers to completing this CMOS design is the need for high drive voltages required to activate the micromirrors bonded above the CMOS module. Unfortunately, the general trend in CMOS design is to create smaller, lower voltage transistors. Therefore, the level shifting circuit in Figure 8-8 was employed to allow dual supply voltages capable of driving integrated micromirrors devices.

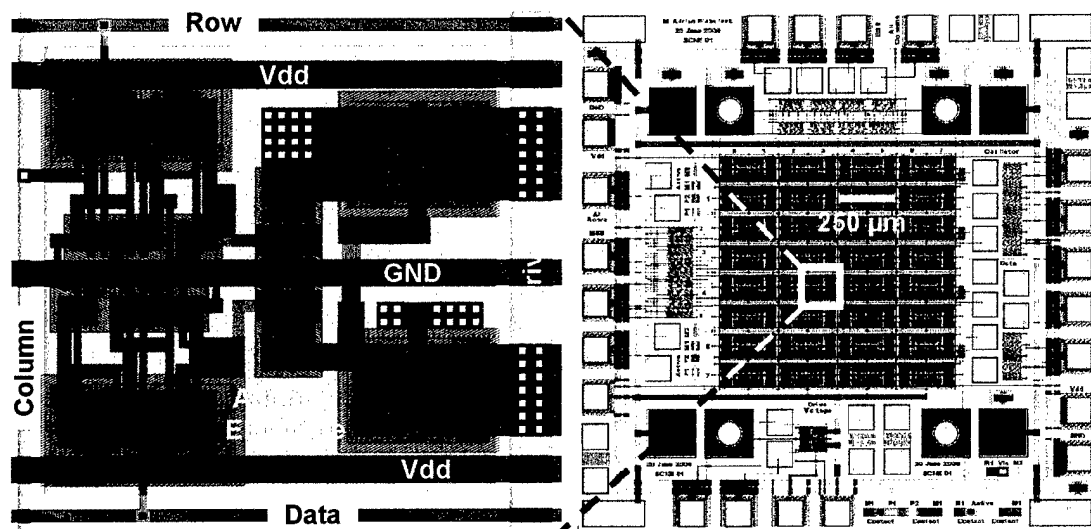


**Figure 8-8.** Symbolic diagram of a level shifting circuit within each address cell.

Using this configuration, the standard 3-5 volt supply is used for all switching and latching functions and a 10-20 volt supply is used for driving the micromirrors. The n-channel transistors are activated by the switching voltage and will pull the

appropriate drain to ground. The corresponding ground that is induced on the opposite p-channel transistor will pull the drain up to the drive voltage. The output drive signal is likewise pulled down to ground whenever the address signal is low.

The layout of this level shifting circuit is shown along the right side of the individual address cell in Figure 8-9(a) under the metal address electrode. Confidentiality agreements prohibit reporting the actual layout with the special layers of the process, but the general layout showing the relative size of the level shifting transistors is evident in this illustration.



(a) Layout of typical address cell      (b) Layout of CMOS receiving module

**Figure 8-9.** Layout of a typical address cell and the full CMOS receiving module.

The latching circuit is shown along the left side of the individual address cell in Figure 8-9(a) with the addition of a single inverter for the true inverse of the address signal,  $A$ , required by the level shifter. The dummy polysilicon spacer layers shown in Figure 8-5 are not shown under the intersection of metal traces in the

corners and along the edges of the cell. To form the complete receiving array shown in Figure 8-9(b), the individual address cells are first mirrored along both axes into blocks of four cells in order to share data and drive lines between all four cells and the appropriate row and column lines between corresponding pairs. That block is then copied into the final 8x8 array in the center of the receiving module. The only other CMOS features relevant to the array are the row and column decoders that are located along the left and top of the array, respectively.

The level shifting transistors are designed with upper polysilicon gates, longer channels and extended drain contacts in order to withstand the higher drive voltage without breaking down. The output of the level shifting transistors is connected to the upper metal address electrode that is patterned above the address cell. This address electrode forms the lower parallel plate that activates the mirror surface of the integrated device. The metal is covered in the last oxide layer of the CMOS process which will insulate the mirror surface when the device is pulled into contact with the CMOS chip. As presented in Chapter 5, this layer of dielectric material adds some complexity to the model of this integrated device.

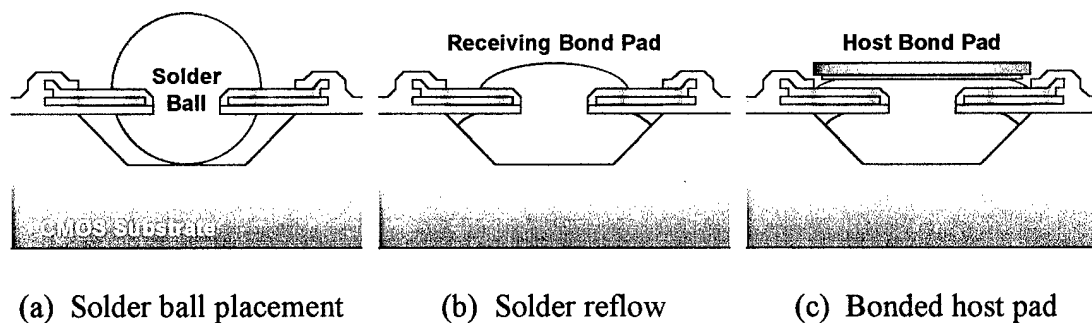
The array of address cells is formed such that a single data line can be shared throughout the array. The row and column address scheme minimizes the control lines to the chip and enables easy JPEG style image encoding for future micromirror tests in which the devices are individually addressed in a zig-zag pattern throughout the array. The common baseline 256-color gray scale palette of the JPEG format is well suited to display applications in which the deflections of the mirror surfaces within the array are simply pulse-width modulated relative to the pixel intensity.

The original CMOS module in Figure 8-9(b) was designed with a variety of test structures. First, the four bond pads were designed with a circular opening in the metal pad to expose the silicon substrate. Bulk etching this area will produce a cavity under the ring of metal which is intended to trap a solder ball once it is reflowed. This option also offers a means to realize accurate self-alignment between the address cells and the array. There are also four similar electroplating pads wired to contacts at each corner of the chip. A small window is cut in the oxide at the center of the pad to electroplate a column of indium upon which the array can be bonded.

Several resistivity and thickness characterization devices are included to extract critical process data for a given foundry service. In order to optimize integrated MEMS structures, the precise topography of the CMOS surface must be well known. Other features such as resistivity of polysilicon and diffusion resistors as well as the true capacitance between polysilicon layers must be accurately measured. In addition, numerous mechanical structures were included to test the ability to locally release such features without a selective post-process etching technique.

Finally, several types of ring oscillators were included to characterize the switching parameters of the cells. In order to obtain the maximum mechanical performance of the array in some applications, the address cells may be refreshed faster than the natural frequency of the micromirror devices. Therefore, the true maximum switching speed for the latching address circuits must be accurately estimated. Since each fabrication run produces a wide variety of electrical parameters that determine the performance of transistors, these ring oscillators and individual test devices are placed in the open areas of every CMOS receiving module.

The original and possibly idealistic approach to bonding the host micromirror array onto the CMOS receiving module is illustrated in Figure 8-10 in which a single solder ball is placed in the center of a bulk etched receiving pad. The precise placement and reflow of such solder balls has been routinely demonstrated at the University of Colorado for the self-alignment and self-assembly of various MEMS components. The inherent characteristics of this technique were intended to produce integrated arrays with minimal alignment error.



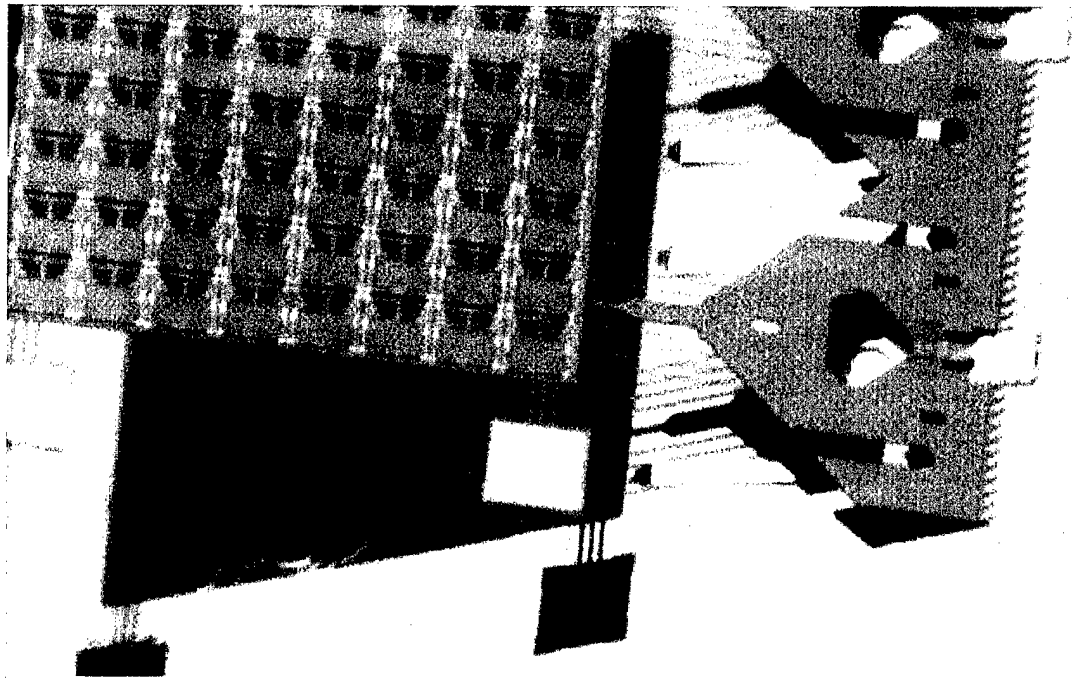
**Figure 8-10.** Illustration of intended solder ball bonding in bulk etched bond pad.

As shown in Figure 8-10(a), the solder ball is placed in the cavity beneath the bond pad that is opened following the bulk etch of the CMOS substrate. The circular holes cut in the center of the metal bond pads are shown in the layout in Figure 8-9(b) over which an oxide window is opened to expose the underlying silicon substrate. Once the solder is reflowed to fill the cavity, the receiving substrate is ready for bonding.

The bond pads connected to the micromirror array were intended to bond directly to the solder which would also bond to the exposed metal of the CMOS bond pads. As illustrated in Figure 8-10(c), the self-alignment capabilities of the molten solder would ideally produce a final integrated array that was near perfectly aligned.

### 8.2.3 Assembly of Flip-Chip Modules

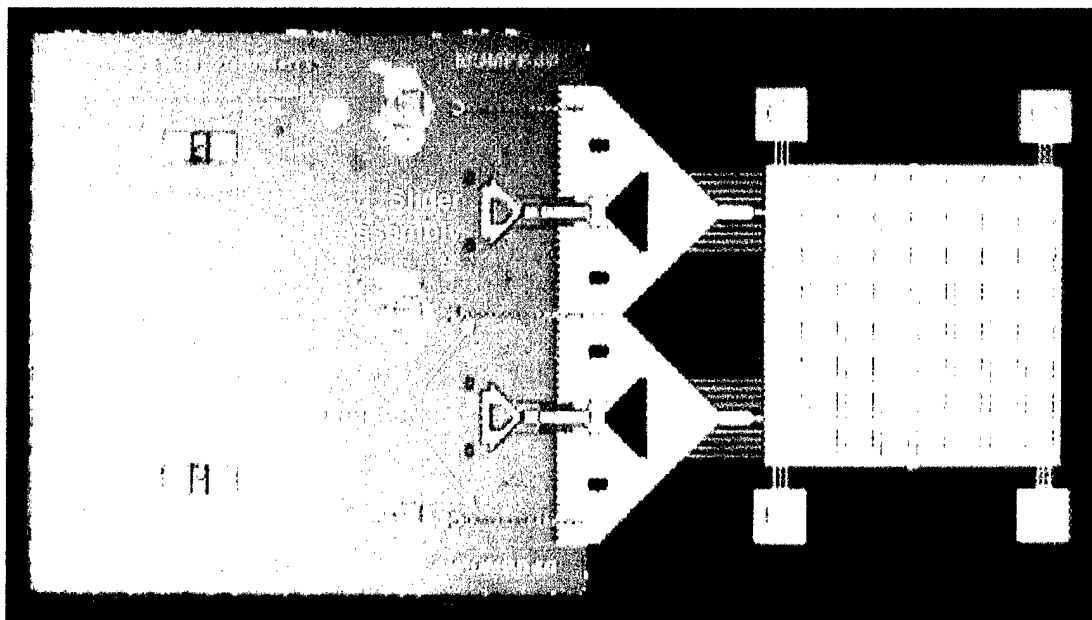
Once the host modules are diced, the arrays must be prereleased so they can be rotated off the edge of the module for CMOS integration. Many of the arrays have tethers or other anchor features that secure the array to the substrate for use in other flip-chip bonding techniques. For integration with CMOS modules, however, these tethers can easily be cut with a laser cutter or simply broken with a probe prior to release. Figure 8-11 shows a typical CMOS integration array after release.



**Figure 8-11.** Photograph of typical micromirror array elevated above host module.

This particular array uses long polysilicon/gold bimorph beams to provide an initial lift to the hinge mechanism. The elevated arrays are much easier to rotate off the edge of the module and can be rotated very simply during the methanol rinse.

Other methods of rotating the mechanism have been explored such as placing large lifting forks under the mechanism which are designed to lift it when pushed with a probe. Although similar forks have successfully erected much smaller features, these forks immediately proved to be a waste of good polysilicon when employed to erect larger structures. Ultimately, only the bimorph lifting beams have demonstrated consistent and reliable rotation of the arrays without damaging devices within them. Although designed with lifting forks, the rotated micromirror array shown in Figure 8-12 was eventually rotated in methanol.

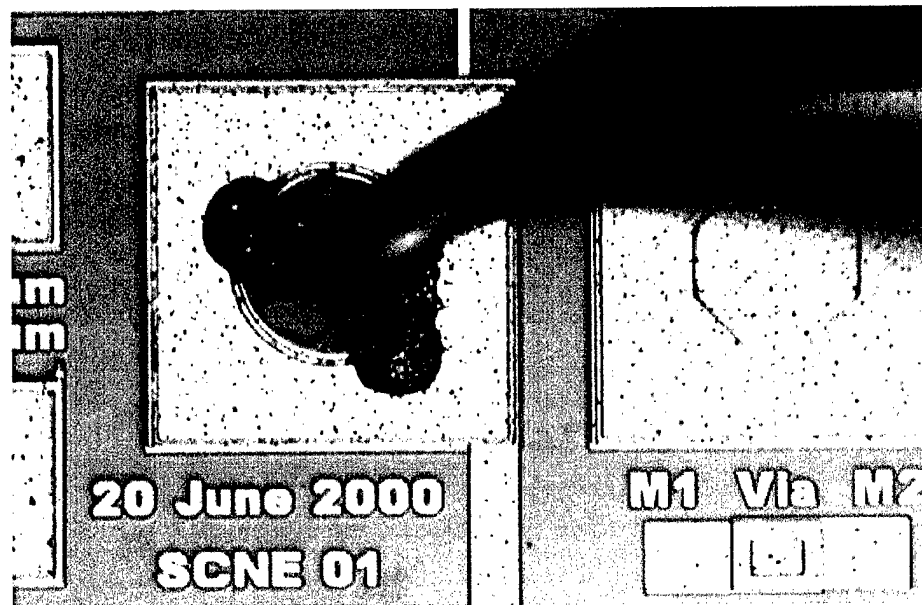


**Figure 8-12.** Released array rotated and latched off the edge of the host module

This array has been latched off the edge of the host module using a probe tip held by hand. One of the unique benefits of this assembly process is that rotated arrays can be metallized or coated with any reflective material of choice without damaging or interfering with the CMOS control electronics or other critical components.



The CMOS receiving module is then prepared with a conductive epoxy which is applied directly to each bond pad using a probe tip. Only a small amount of epoxy is needed to effectively bond the planar surfaces of the opposing bond pads. As shown in Figure 8-13, circular holes in the bond pads are designed to receive matching dimples in the host bond pads in order to reduce alignment error.

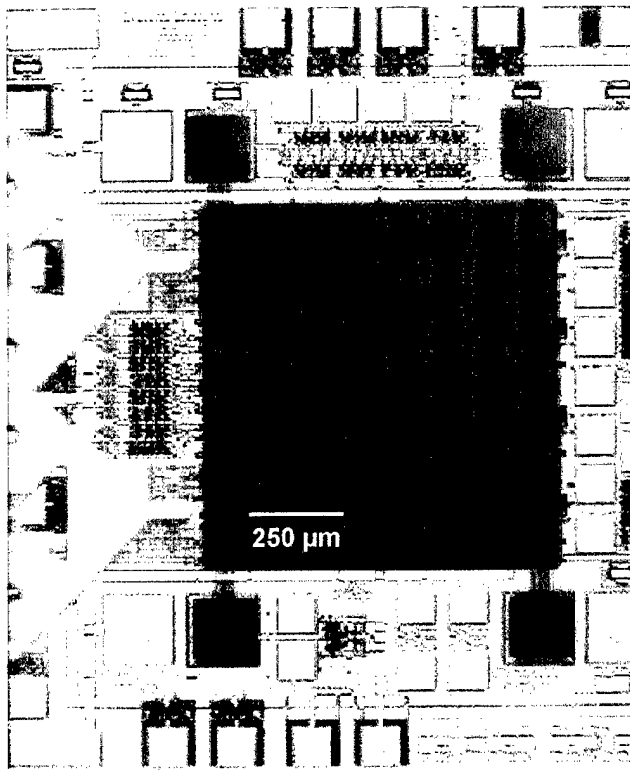


**Figure 8-13.** Photograph of conductive epoxy applied to CMOS receiving module.

These holes in the center of the bond pads are also used to enable bulk etching of the substrate and to catch excess epoxy to prevent bonding errors. Although a number of conductive epoxies could be used, the Magnobond 8007 single component epoxy from Magnolia Plastics, Inc. seemed to produce the best results.

The host module is affixed to a micromanipulator by a variety of techniques such as a custom chuck containing a flat surface which holds the module by epoxy, tape, or contact surface. As rudimentary as it seems, attaching the host module to a

flexible wire using fast curing epoxy is the most reliable technique and also allows for course alignment. As shown in Figure 8-14, the array is positioned over the receiving module and aligned using probe station tilt, rotation and translation controls.



(a) Alignment of array over CMOS module

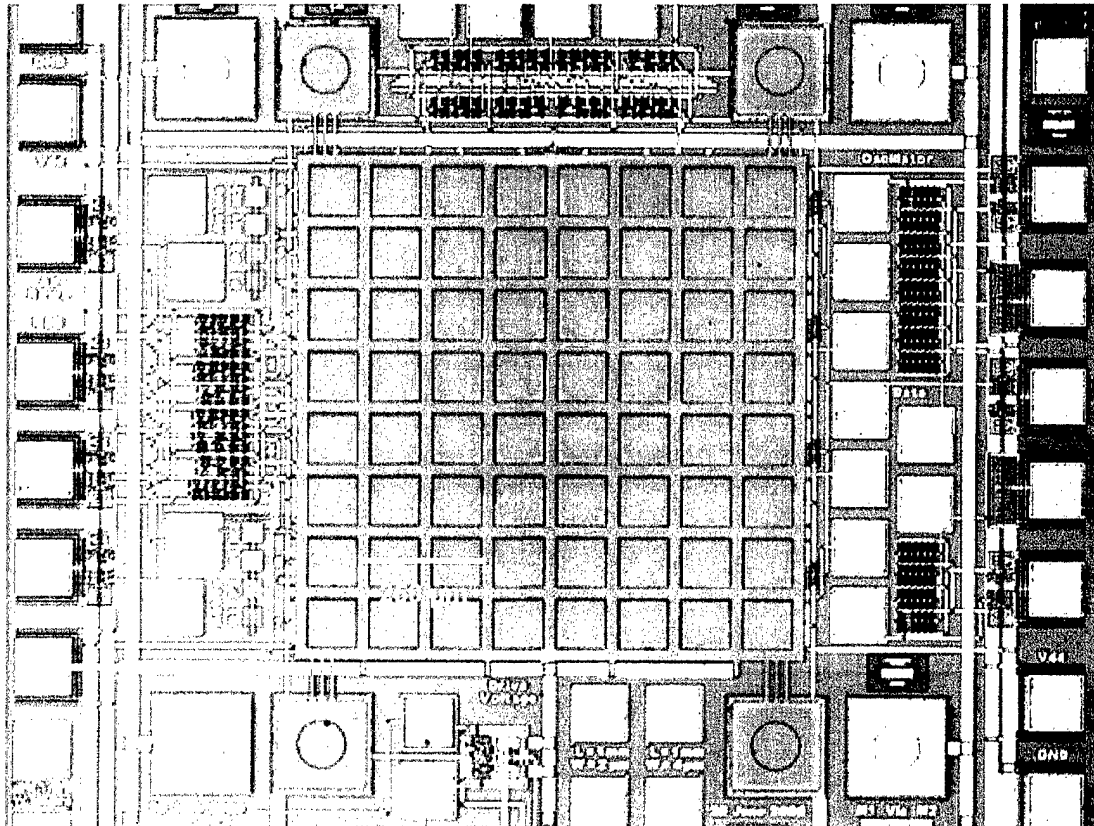


(b) Photograph of Juan Valdez

**Figure 8-14.** Alignment of typical micromirror array over CMOS receiving module.

Course alignment is performed using the stage controls to adjust lateral position and rotation while fine alignment is performed using the micromanipulator controls. Although the micromanipulator does not have rotation adjustment, the precision of the stage rotation was more than sufficient to align the arrays. The planar orientation of the arrays to the receiving modules is surprisingly easy to determine from the lighting and relative focus while viewed through the probe station microscope.

After sufficient alignment is achieved, the bond pads of the array are pressed into contact with the epoxy on the bond pads of the CMOS receiving module. As shown in Figure 8-15, the flip-chip tethers that support the array are then severed to produce the final integrated micromirror array on the CMOS receiving module.



**Figure 8-15.** Photograph of a typical integrated micromirror array.

Although the hinge mechanism is designed to latch the array into a position that is rotated  $180^\circ$  from the fabricated position, there have been several cases in which the arrays were held at  $90^\circ$  to facilitate bonding. Several modules have been observed to be significantly larger than the drawn dimensions due to poor alignment during dicing. As a result, the arrays attached to the hinge mechanism sometimes do

not reach the center of the CMOS receiving chip before the edges of the two modules make contact. One solution would be to enlarge the host modules so that the tethers supporting the array could be lengthened. Unfortunately, this approach uses significantly more area of the MUMPs chip.

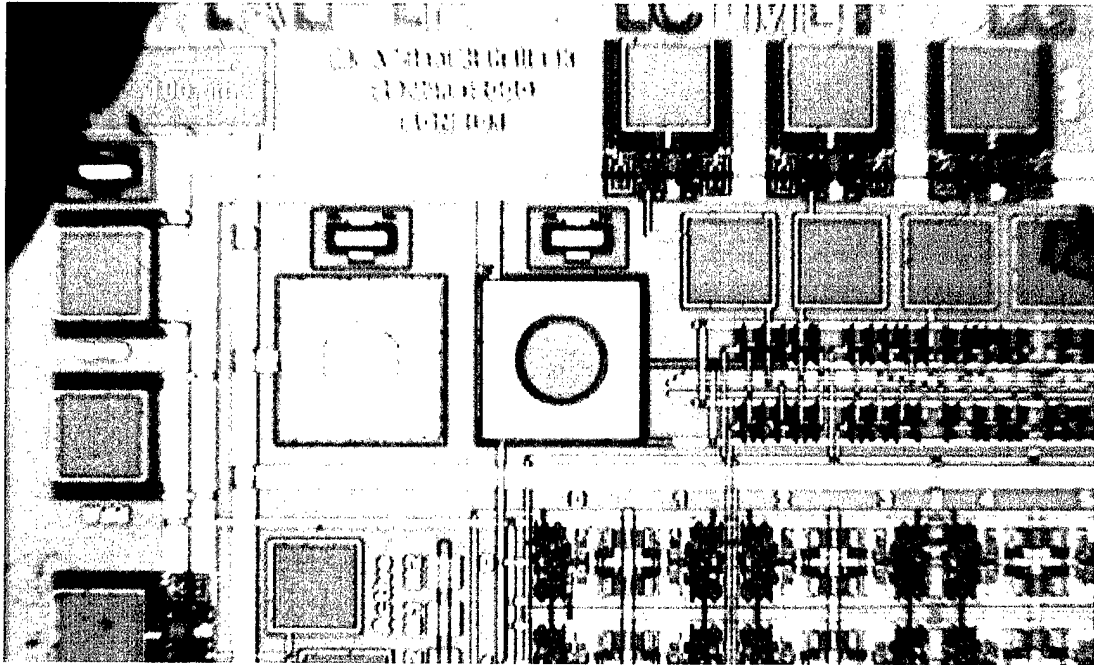
Another solution is to design new CMOS receiving modules in which the address cells are positioned along the edge of the chip. For the current modules, however, an effective solution is simply not to latch the hinge mechanism, but to allow the array to hang beneath the host module and draw it along the surface of the receiving module. This technique, however, requires significantly more care for alignment and avoiding premature contact with the conductive epoxy deposited on the bond pads. Attempting large position adjustments after such contact usually results in lost or damaged pads.

### **8.3 Yield Analysis**

Given the small number of integrated arrays produced, there is little data to support a full yield analysis. Of the larger number of arrays that were rotated for this and other flip-chip applications, however, approximately 80% were successfully deployed with no damage or contamination to the arrays. Although the application of epoxy to the CMOS module and final bonding of the arrays demonstrated no failures, some arrays did show adverse effects if the epoxy was not immediately cured. Ultimately, poor CMOS fabrication resulted in the worst yield of the process in which only 30% of all electronic and mechanical structures functioned as designed.

### 8.3.1 Reliability of CMOS Fabrication

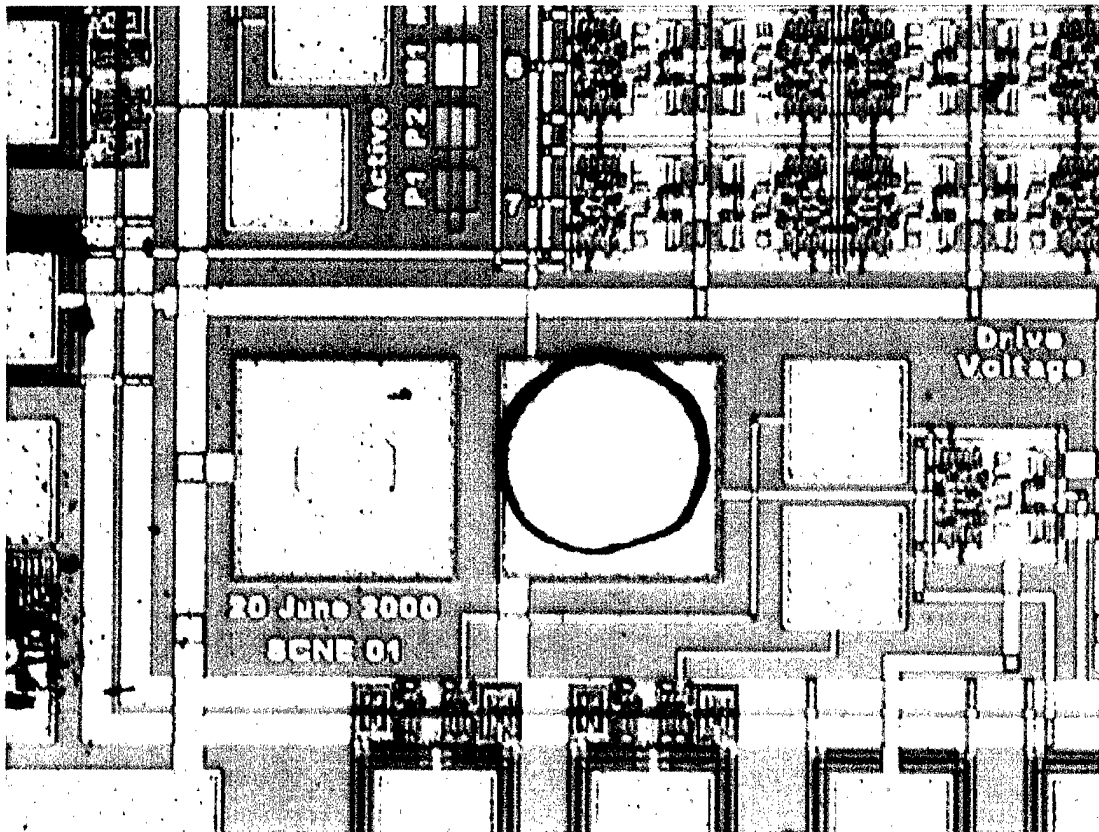
One of the disappointing aspects of this research stems from reliability issues in the fabrication of the receiving modules. The first sets of CMOS chips demonstrated a variety of adverse characteristics such as unexposed metal on bond pads that supply the ground channel to the integrated arrays. Figure 8-16 shows one such module that has been bulk etched in EDP to open a cavity beneath the pads.



**Figure 8-16.** Photograph of bulk etched CMOS module showing shielded pads.

After an excessively long etch, the corners of the substrate and the exposed metal on probe pads had been completely removed, but the bond pads remained fully formed. Although the oxide cuts are evident above the pads, it is apparent that some oxide remains on the surface of the metal which makes electrical and mechanical contacts with the arrays very difficult if not impossible to achieve.

The effect of this fabrication error can be seen when attempting to apply solder to the CMOS receiving module for micromirror integration. Before the arrays were bulk etched, several 4 mil Sn/Pb solder balls were placed on the pads and flattened using a glass slide. As shown in Figure 8-17, the solder covered the majority of the surface area of the pad and should easily bond to the exposed metal.



**Figure 8-17.** Photograph of attempted solder ball reflow on CMOS bond pads.

Unfortunately, the solder merely formed the original ball upon each reflow indicating that the solder was not bonding to the metal pad. Resistivity probes later confirmed the electrical isolation of the pads. As a result, the pads had to be scraped with a probe tip to expose the metal before the conductive epoxy was applied for bonding.

Some of the receiving modules demonstrated other adverse features such as diode effects in diffusion resistors, various digital logic faults and level shifting circuits that simply could not survive the higher drive voltages suggested by the foundry. Furthermore, many of the logic gate standard cells that have been successfully used for many years in other CMOS foundry services produced a wide variety of results. Some address control lines from the column decoders failed while the identical cells that were copied into the row decoders worked properly.

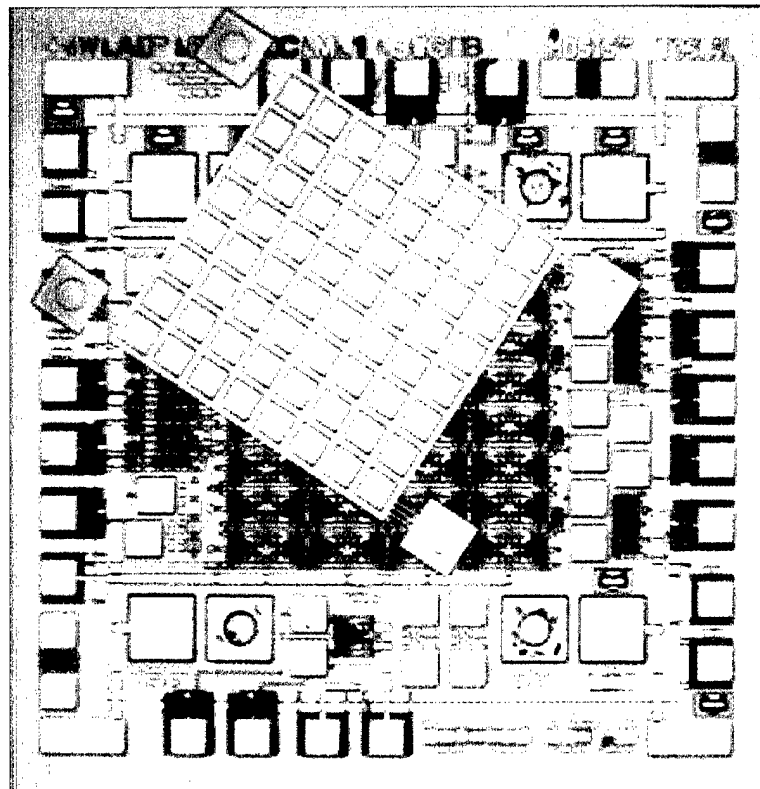
### **8.3.2 Damage to Rotated Arrays**

Although the majority of micromirror arrays were successfully released and rotated off the edge of the host module, there were many typical mechanisms by which the process could fail. The primary concern for the arrays was during the release itself. As discussed in the previous chapter, a galvanic cell formed in the HF solution between the gold pads on the bonding frame of the array. As a result, the surface of each device, its flexures, and the bonding frame itself were damaged as the dopant atoms were selectively etched to form porous polysilicon. Additionally, the resulting residue covering many devices often created stiction problems as the surfaces stuck to the substrate and broke off the bonding frame during rotation.

Also discussed in the previous chapter was the formation of oxide columns between the surface of each device and the substrate. As the oxide is removed from within the device, a column of oxide beneath the surface is often the sole anchor of the array connected by the flexures of the device. As a result, any agitation to the HF solution to prematurely rotate the array poses the risk of damaging some devices.

### 8.3.3 Conductive Epoxy Drift

Although all of the original arrays were successfully assembled using the hinge mechanism, some of the arrays began to shift when the epoxy supporting them was not immediately cured. Figure 8-18 shows one such array that eventually drifted off the receiving bond pads during testing.



**Figure 8-18.** Photograph of unsecured array atop CMOS receiving module.

Over a period of several hours, the epoxy either partially evaporated or spread too thin to support it the micromirror array. Traces of remnant epoxy can be seen on the three CMOS receiving bond pads that are still visible in the photograph. As a result, it was found that the conductive epoxy should be cured immediately after bonding.

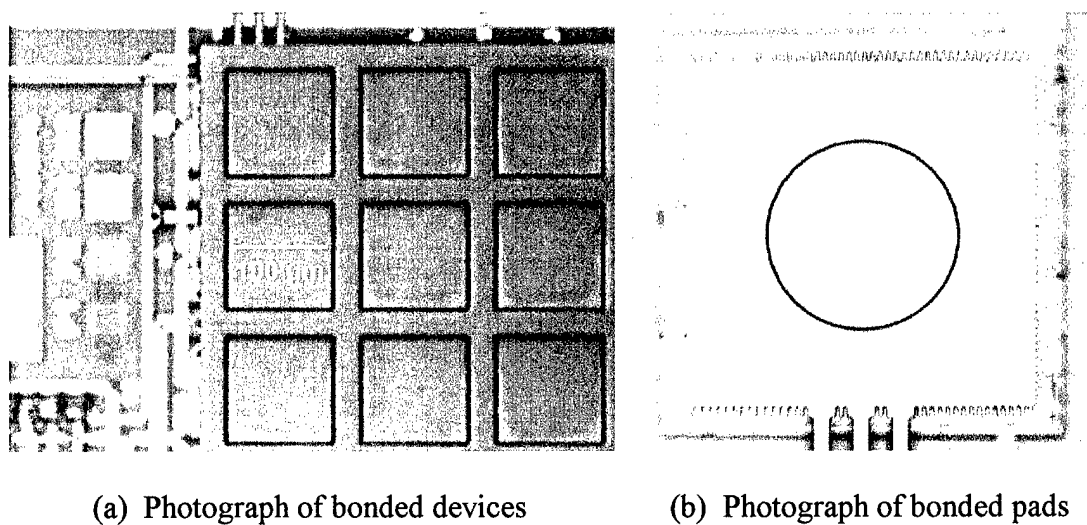


## 8.4 Device Performance

Although this portion of the flip-chip research was originally the main priority of the sponsor, it was very quickly dismissed and replaced by the submount bonding once that technique was demonstrated. As a result, only some of the initial arrays were thoroughly tested. This section reports the bonding and limited testing results.

### 8.4.1 Bonding Characteristics

One of the most surprising aspects of flip-chip integration is the simplicity with which the arrays were bonded to the CMOS modules. As shown in Figure 8-19, the arrays were successfully bonded with very little alignment error between modules.

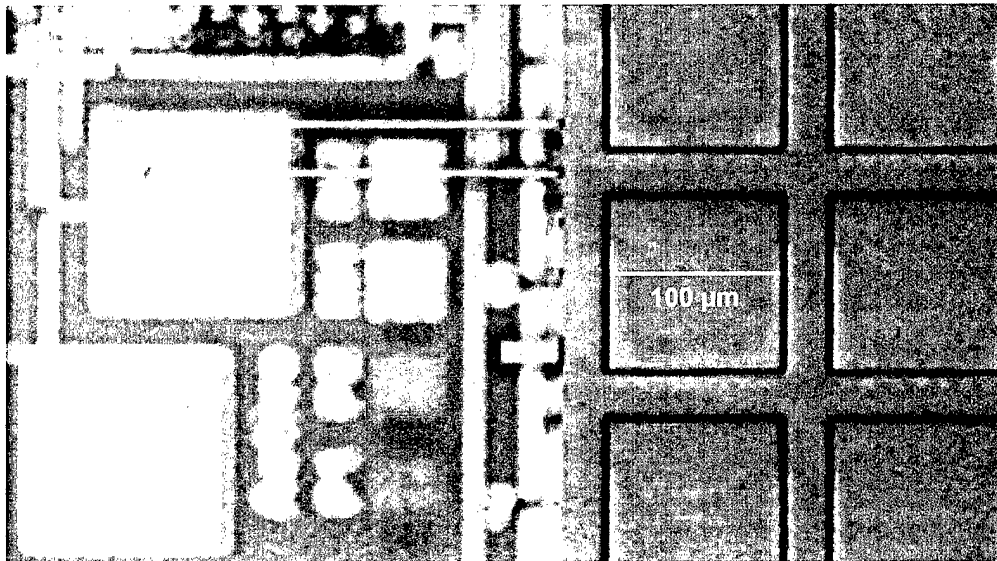


**Figure 8-19.** Photographs of bonded features showing nearly ideal alignment.

The micromirror devices shown in Figure 8-19(a) were positioned directly above the corresponding address electrodes fabricated on the CMOS module with no apparent

rotation or lateral alignment error. To quantify any such error, a series of 2  $\mu\text{m}$  scales were distributed with 2  $\mu\text{m}$  spacing around the outer edge of the bond pads. As shown in Figure 8-19(b), the alignment of the micromirror array atop the CMOS module appears to be roughly 1  $\mu\text{m}$  or less. Given that the alignment is performed manually, it is obvious that the alignment tolerance is simply a matter of personal preference driven by the application at hand.

The only noticeable problem with the flip-chip integration using the off-chip hinge mechanism is that some of the tethers did not break as desired and left remnant beams supported by the array. As shown in Figure 8-20, the tethers do not alter the operation of the array, but may interfere with features surrounding it.



**Figure 8-20.** Photograph of integrated array with remnant tethers over probe pads.

These tethers were designed with stress concentration points attached to the bonding frame around the array to ensure they break along the edges of the array. Although

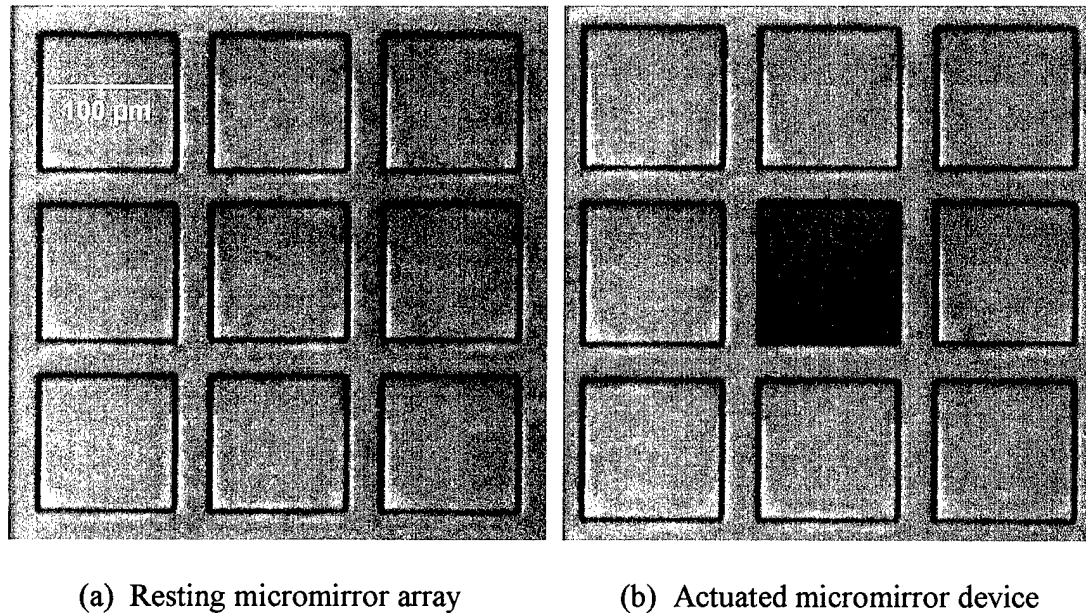
most of the tethers broke at precisely the desired location, these tethers appear to have been severed from the off-chip hinge mechanism during rotation of the micromirror array. Rather than risk contamination of the array by removing them, the tethers were left attached to the frame of the array.

The conductive epoxy was cured by placing the bonded microsystem on a heated stage set at 100°C for roughly one hour. To minimize the effect of shifting during this process, the temperature was slowly increased from room temperature over a period of 15 minutes. Although the time to cure the epoxy could be reduced by increasing the temperature, the delicate transistors on the CMOS module could be damaged as charge carriers diffuse out of highly doped wells at higher temperatures. Tests on the CMOS modules before and after curing suggested that the elevated temperature was not the cause of failure for many of the electronic circuits.

In general, the integration of the arrays was quite successful. Each device within the array was designed with minimal gold spacer pads surrounding each device in order to reduce curvature within the array. Additionally, small via staples between the two polysilicon layers of the bonding frame were distributed around each device and across the entire array to stiffen the frame. Although the bond pads displayed significant warping due to thermal mismatch stress between gold and polysilicon layers, they are connected to the arrays via long flexures that are designed to isolate this surface variance. As a result, each of the arrays displayed no more than 120 nm of total surface variance across the 1 mm square active surface area. Several arrays were characterized immediately after curing the epoxy and then again characterized several months later. The arrays showed no signs of shifting or warping in that time.

#### 8.4.2 Device Behavior

The cantilever devices were designed to operate in a binary mode in which the surfaces are either fully deflected or resting in the plane of the bonding frame. Provided the CMOS address cell could survive the drive potential, the devices typically deflected as desired. Figure 8-21 shows a typical cantilever micromirror device that deflects to roughly  $3.1^\circ$  of tilt with a 10.2 volt drive potential.

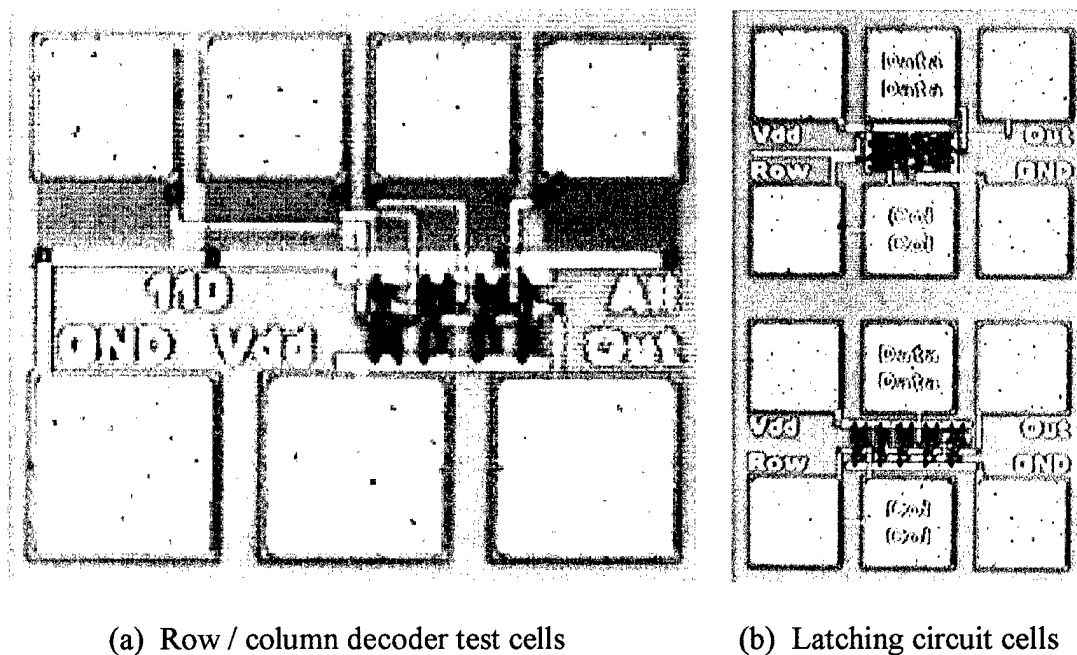


**Figure 8-21.** Photographs of typical integrated micromirror device actuation.

Although the devices appeared to immediately return to the resting position when the address cell was deactivated, no high frequency tests were conducted to quantify any possible effects of charging in the upper oxide layer of the CMOS module. Some micromirror designs required a drive potential that was greater than the level shifting circuit could withstand and many of the drive circuits were destroyed.

A characteristic model for these integrated micromirror devices was developed in Chapter 5 by equating the electrostatic torque induced by the address electrode with the restoring torque of the flexures. Ideally, these devices could be tested to validate the model by measuring the angle of rotation for stable deflections at various address potentials. Unfortunately, the level shifting circuit demonstrated somewhat inconsistent behavior at low address potentials and whenever the drive potential was modified while the address cell was latched in the active state.

Numerous cells fabricated on the CMOS modules were also tested to validate the performance of the electronics. Figure 8-22 shows some typical test cells.

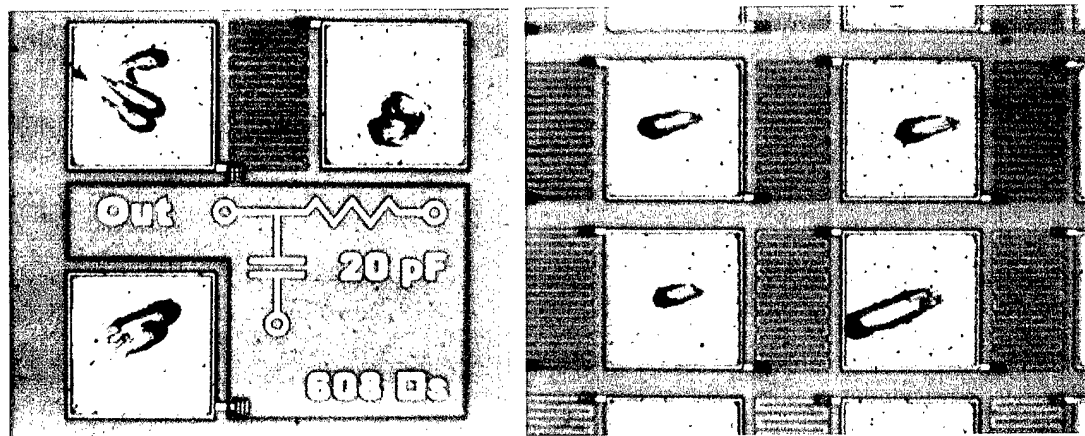


**Figure 8-22.** Photographs of typical isolated critical circuit test structures.

A portion of the row/column decoder array is shown in Figure 8-22(a) in which several “pull-down” probe pads were used to simplify the testing process. Likewise,

various designs of the latching circuit are shown in Figure 8-22(b) in which identical standard logic gates were fabricated in close proximity and widely spaced. Although the design rules of the process indicated that the close proximity was allowable, these test cells produced different results. Repeated tests on a variety of test cells indicated poor fabrication and reliability in the CMOS electronics.

At the time the original CMOS modules were designed, numerous other microsystems were intended for demonstration of the flip-chip integration process. In order to provide critical data for future projects, several passive test structures were also studied. Figure 8-23 illustrates some of these test structures.



(a) Typical passive filter element

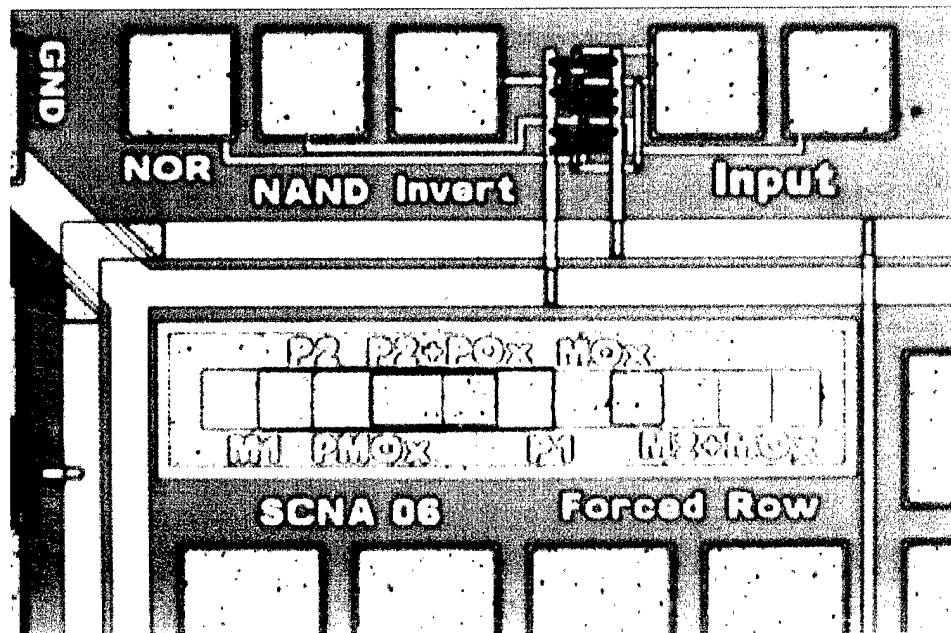
(b) Polysilicon resistor chain

**Figure 8-23.** Photographs of typical passive test elements on CMOS modules.

The true value of capacitance between polysilicon layers and the resistivity of polysilicon wires are somewhat important when designing integrated microsystems such as Hall effect magnetometers and digital/analog converters. The filter element in Figure 8-23(a) provided nearly ideal data for future use in frequency analysis as did

the resistor chain in Figure 8-23(b) which would eventually be used as a voltage divider for mixed signal conversions. Other passive test structures such as diffusion resistors and various isolation regions were also tested with favorable results.

As previously described, the layer thickness data for the CMOS process is very important when designing the mechanical devices that will be bonded above any topography induced in the surface of the module. Since the foundry refused to divulge this information, the layer test structure in Figure 8-24 had to be designed.



**Figure 8-24.** Photograph of a typical CMOS module layer test structure.

Beneath the upper metal layer, various combinations of lower layers are designed to induce topographical effects in the surface. Sufficient layer combinations are designed to extract the thickness of each individual layer offered by the foundry. The oxide layer over the metal must be removed to allow interferometric characterization.

Since a new CMOS fabrication service is highly recommended for future integration, the results of these tests are not reported. Instead, similar structures should be included on future modules fabricated in a more reliable CMOS process. Ultimately, the performance of the integrated microsystem is most significantly influenced by the quality of the design and fabrication of the CMOS module.

## **8.5 Conclusions**

The latching off-chip hinge mechanism has enabled reliable, fast, simple and low-cost integration of MEMS structures bonded directly atop CMOS electronics. Both the MEMS host module and corresponding CMOS receiving module can be commercially prefabricated in a variety of existing foundry services that are optimized for reduced cost and rapid delivery. Using the off-chip hinge mechanism, virtually any MEMS structure can be prereleased and then rotated and latched off the edge of the MEMS host module for integration with CMOS receiving modules. Structures rotated off the host module can be easily metallized or coated with virtually any desired material without masking procedures or adverse effects on the host structures or receiving module.

Although most of the integrated microsystems displayed disappointing CMOS performance, the integrated arrays presented in this section clearly demonstrated the simplicity with which similar integrated microsystems could be created. Ultimately, the flip-chip integration of MEMS on CMOS electronics using the off-chip hinge mechanism has proven to be a viable means to assemble such systems.



## **CHAPTER 9**

### **BROAD DESIGN CONCEPTS**

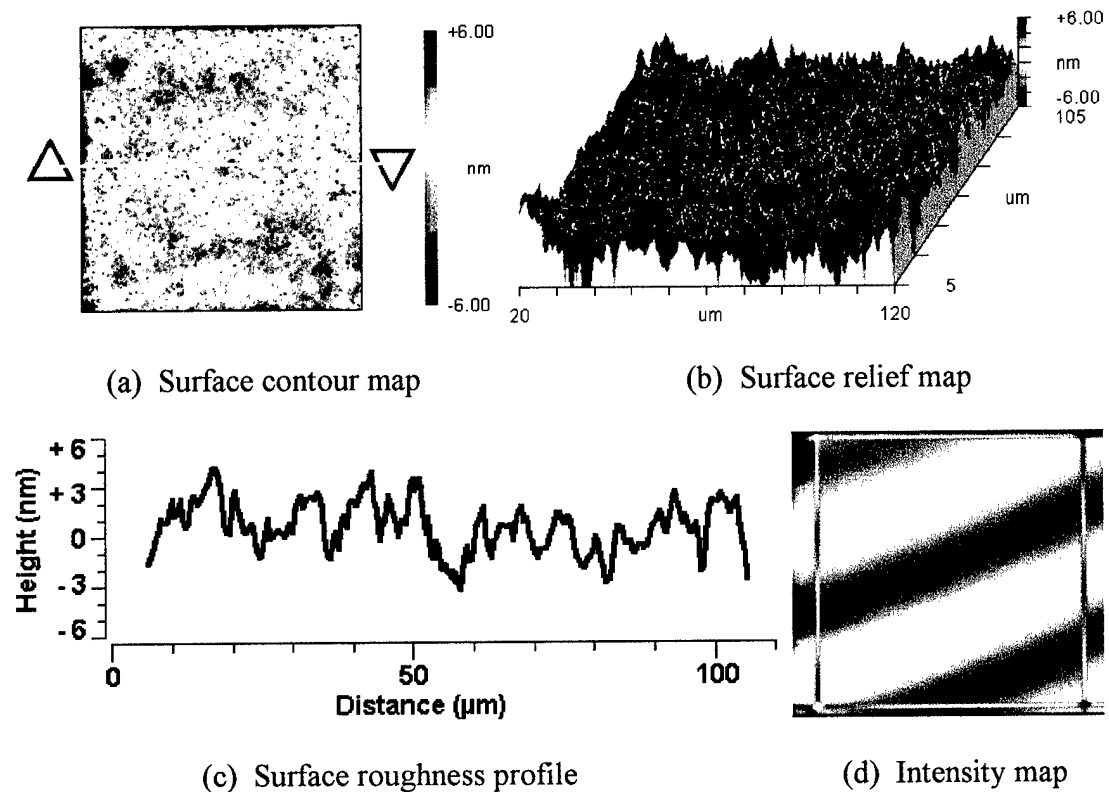
This chapter describes several advanced concepts that are shared by a variety of the flip-chip assembly techniques presented in previous chapters. Since none is specific to any one form, these concepts are presented as universal features or methods that can be employed in flip-chip bonding. For instance, the inherent planarization of flip-chip structures is a benefit shared by all structures fabricated on ceramic substrates, submount modules, or CMOS electronics. As a result, a statistical analysis of observed surface roughness is presented as a universal flip-chip concept.

#### **9.1 Inherent Planarity of Flip-Chip Structures**

One of the most important features of a micromirror device is the local planarity and reduced roughness of the mirror surface. The flip-chip assembly process inherently produces almost ideally flat mirror surfaces due to the inverted nature by which they are fabricated. The mirror array is designed upside down on the host substrate with the mirror surface being the underside of the first releasable layer. Since it is fabricated directly on a flat layer of oxide, the mirror surface is formed in a highly planarized polysilicon layer that becomes the upper layer of flip-chip devices.

### 9.1.1 Baseline Surface Roughness Characterization

The Zygo interferometric microscope was used to study the reflective surface area of a large number of micromirror devices. Using a high magnification objective, surface roughness data could be directly collected from individual micromirrors. Figure 9-1 shows a surface characterization of a typical 100  $\mu\text{m}$  square flip-chip micromirror device and demonstrates the optically smooth nature of the surface.



**Figure 9-1.** Surface roughness characterization of a typical flip-chip micromirror.

The vertical scales of the plots in Figure 9-1 are extremely exaggerated to show the surface of the device. As illustrated in Figure 9-1(b), the peak deformation or surface variance across the device is approximately 12 nm over the 100  $\mu\text{m}$  square surface.

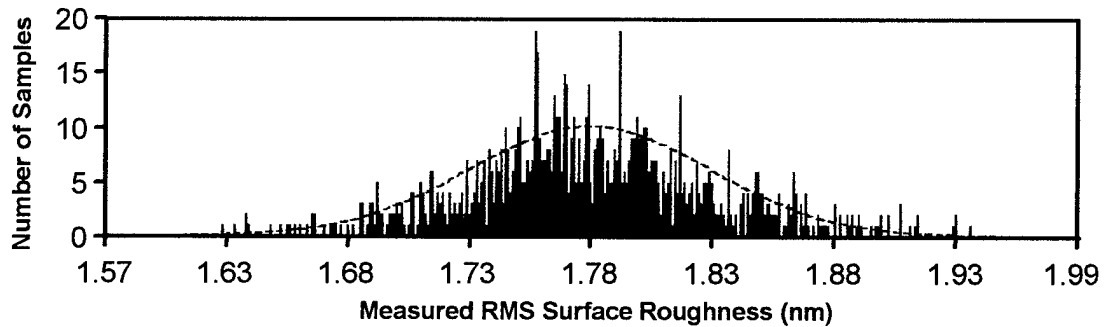
This unprecedented quality in the mirror surface could only be duplicated by adding very costly and complex steps to existing surface-micromachining processes [2]. Figure 9-1(a) shows the surface contour plot of the surface roughness data through which the deflection profile lines can be drawn to obtain specific surface roughness. This surface roughness profile is shown in Figure 9-1(c) which illustrates a typical peak-to-valley surface variance of only 7-8 nm observed across 100  $\mu\text{m}$  devices with an average of only 1.6 nm of RMS roughness throughout the arrays.

The surfaces of each micromirror are so flat that no radius of curvature could be extracted from the surface relief data. The surface profile through the center of a typical micromirror in Figure 9-1(c) demonstrates the optically smooth and flat nature of the reflective surface of a flip-chip micromirror. In comparison, even the most advanced planarized commercial process in the country typically demonstrates more than 150 nm of print-through topography in micromirror surfaces [2].

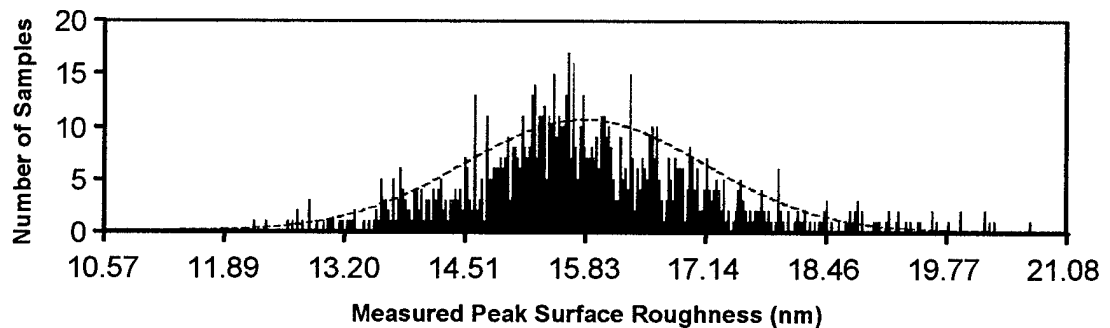
### **9.1.2 Statistical Study of Surface Roughness**

Because the mirror surface of flip-chip micromirror devices is originally fabricated on the surface of the first oxide layer on the host module, the mirrors are typically very planar in nature and demonstrate only minor deformations. The planarity of cantilever devices was studied using the Zygo interferometric microscope by characterizing a large sample of micromirror devices over several months of high-volume flip-chip bonding. A sample of 1000 identical 100 x 100  $\mu\text{m}$  mirror surfaces was measured for RMS and peak surface roughness data.

The average RMS surface roughness of the sample set was only 1.779 nm with a 0.051 nm standard deviation and the average peak surface roughness was only 15.828 nm with a 1.314 nm standard deviation. Figure 9-2 shows the normal distributions of the measured RMS and peak surface roughness data.



(a) Measured RMS roughness data for N=1000 devices



(b) Measured peak roughness data for N = 1000 devices

**Figure 9-2.** Normal distribution of measured RMS and peak surface roughness data.

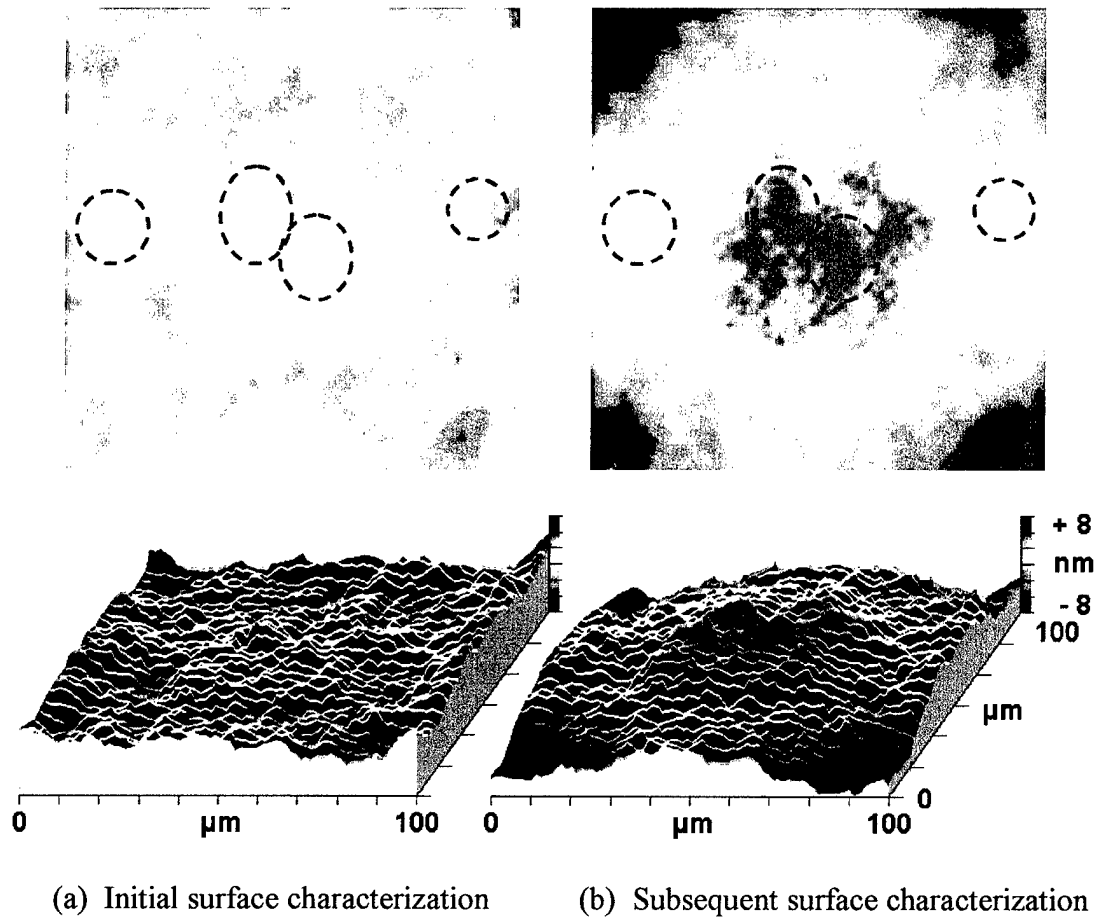
Although Figure 9-1 shows a maximum vertical plot range of only 12 nm, most devices had very localized spikes that accounted for the total peak variance. Since these spikes rarely appear on any of the surface plots, it is likely that even these values are numerical aberrations that produce values much greater than the true surface roughness data provided by the computer.

The RMS algorithm naturally averages the roughness of the mirror surface and tends to be less affected by highly localized deformations. As a result, the data shown in Figure 9-2(a) is closely and evenly distributed about the mean. A variety of minor spikes in the mirror surfaces, however, produce the slightly uneven distribution in Figure 9-2(b) which shows that many surfaces with highly localized aberrations produced somewhat higher peak roughness data. Based on these results, however, it is clear that flip-chip surfaces demonstrate remarkable planarity that rivals even far more costly fabrication services [5].

It is interesting to note that there was no apparent correlation between a particular peak measurement and the relative measurement of RMS roughness for a particular device. Since the peak values were based on highly localized deformations in the surface, a device with a very large relative peak roughness could still display a smaller relative RMS roughness.

Some of the same mirror surfaces initially characterized in this sample set were again characterized several months later. The initial surface contour and relief map in Figure 9-3(a) show that the device demonstrates only minor surface roughness features resulting in the measured RMS and peak surface roughness data of only 1.723 nm and 14.837 nm, respectively. The subsequent characterization shown in Figure 9-3(b), however, indicates that the mirror surface creeps slightly and now displays some noticeable downward curvature. The measured RMS and peak surface roughness data are now 3.249 nm and 24.615 nm, respectively. The rate of change in the surface is not known since only the two characterizations were made several months apart. However, it is reasonable to assume that the variations in

environmental conditions over the transition from winter to summer and the resulting heating and cooling of the laboratory gradually influenced the transformation.



**Figure 9-3.** Initial and subsequent surface characterization of a flip-chip device.

Although some specific data point in the surface characterization produces the larger peak roughness, it should be noted that the total vertical plot range in Figure 9-3(b) is only 16 nm and shows no apparent saturation of the data. Further study is required to determine if this value truly represents the actually peak deformation in the mirror surface or whether the results are subject to numerical aberrations in the data.

The surface relief plots shown in Figure 9-3 illustrate the precision of the Zygo interferometric measurement system where the vertical scales in these plots are highly exaggerated relative to the lateral dimensions of the mirror surface. Many of the same surface features apparent in Figure 9-3(a) are also visible in Figure 9-3(b) after the surface has deformed slightly which demonstrates remarkably consistent representation of the mirror roughness. For instance, the relative minimum in the surface shown in the lower right corner of the surface contour plot in Figure 9-3(a) is likewise represented as the lowest point in the surface shown in Figure 9-3(b) after the corners have deflected. The relative maximum at the center of the device and also in the upper right corner are also consistently represented between measurements. It is important to note that the vertical change in surface variance is only 10 nm across the 100  $\mu\text{m}$  square surface of the mirror. Even after such deformation, the mirror surface demonstrates roughly a 0.62 m radius of curvature.

## **9.2 Off-Chip Latching Hinge Mechanism**

This section presents the design, fabrication and implementation of a novel off-chip hinge mechanism that can be latched in place to hold surface-micromachined structures off the edge of the chip. This mechanism was designed to enable fast, reliable, accurate, simple, and low-cost fabrication of advanced flip-chip MEMS structures. The upper layers of a flip-chip device can be commercially prefabricated on a host module attached to the hinge mechanism while the lower layers can be prefabricated on virtually any desired receiving module.

This section presents the fabrication of a variety of advanced micromirror arrays assembled using this mechanism. This research demonstrates that structures comprised of several surface-micromachined layers can be positioned and bonded onto a variety of work surfaces such as ceramic substrates, MEMS chips and even CMOS electronics using adhesives, solder, gold bonding or mechanical latches. The hinge mechanism is designed to be easily disabled by a variety of methods should another bonding technique be desired. All flip-chip modules are designed with the mechanism to enable multiple flip-chip assembly options.

### **9.2.1 Motivation**

Throughout the course of this research, many of the flip-chip devices have been assembled and tested independently without concern for an underlying technique that may be more universally applicable to a wider range of devices. The future direction of this research should incorporate the development of such a technique. In short, the purpose of this research is to develop and demonstrate a simple, reliable, repeatable, and inexpensive post-process assembly technique that would make use of existing commercial fabrication services.

In order to be a significant contribution to the field, this new flip-chip assembly technique must overcome all of the adverse effects demonstrated in devices assembled using the current flip-chip assembly technique. For that reason, any new technique must be universally applicable to nearly all MEMS structures, must not require specialized equipment such as the flip-chip bonding machine, must inherently minimize alignment errors and should involve little or no complex preprocessing.

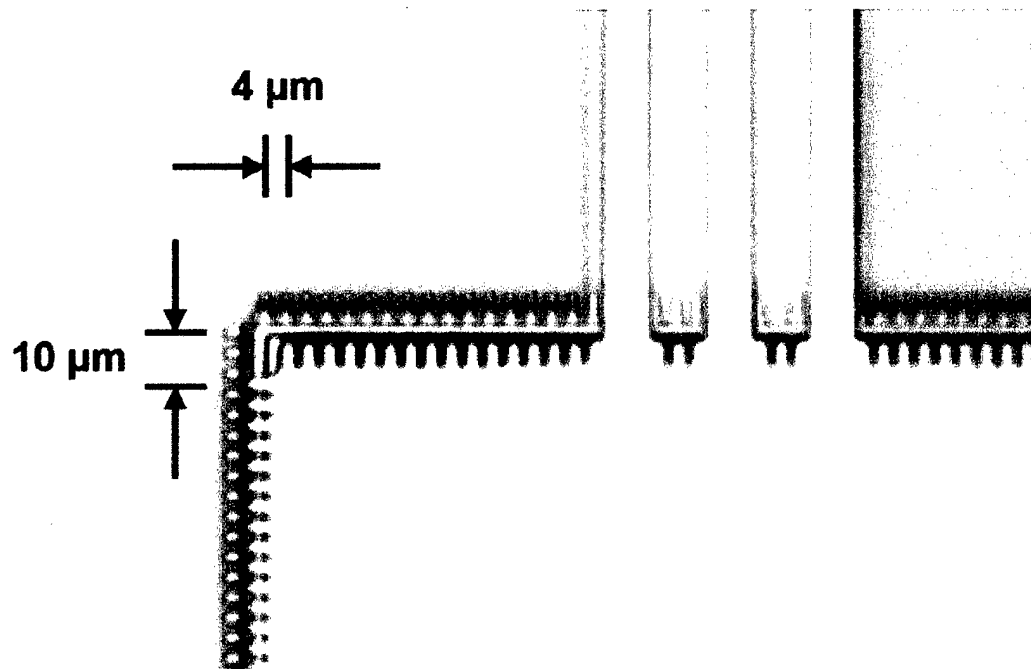


The primary disadvantage of the baseline flip-chip assembly technique is the alignment error between the host and receiving modules that is inherent when using the flip-chip bonding machine. The primary cause of misalignment is the camera system used to superimpose the image of the two modules. The beam splitter is positioned on a translation platform to be adjusted when calibrating the camera system. A significant error can be induced each time the camera assembly is moved into position and then withdrawn from the bonding area for each bonding cycle. The mechanical tolerance of the bearings supporting the camera assembly propagate to a positioning error between flip-chip modules of roughly 10  $\mu\text{m}$  or more if the camera system is not calibrated after only a few cycles.

Another source of alignment error is the mechanical tolerance of the other moving components of the machine. These large-scale components are designed with very precise specifications and intended to position micromachined devices with as little error as possible. Unfortunately, the camera system must be inserted between the two modules which forces a separation distance of roughly 10 cm during alignment. After the host module traverses that distance, the alignment is occasionally compromised to the extent that the transferred structures are sometimes unusable or the bond does not hold.

Without repeated calibrations, the bonding machine typically produces an alignment error of approximately 8-15  $\mu\text{m}$  and shows a wide variance in the direction of error. Although this error can be reduced to 1-3  $\mu\text{m}$  with repeated calibrations, the alignment error will always remain a primary concern. The net alignment error induced by both sources can be seen in Figure 9-4 which shows a bonded pair of

typical pads having alignment marks distributed around the edges. These alignment marks are  $2\text{ }\mu\text{m}$  wide with  $2\text{ }\mu\text{m}$  spaces and indicate the bonded structure was misaligned by the dimensions shown.



**Figure 9-4.** Photograph of bonded flip-chip pads showing extreme alignment error .

In order to overcome this alignment error, a new technique was developed to allow designers to assemble flip-chip structures without highly specialized bonding equipment and with little or no complex preprocessing. In short, the use of the latching off-chip hinge mechanism has proven to be as fast, simple, and inexpensive as the standard flip-chip bonding process, but with none of the disadvantages. Virtually any flip-chip structure can now be transferred to any desired substrate using only common equipment and without damage during release.

The advent of the latching off-chip hinge mechanism significantly increases the yield to a point where rapid prototyping and some commercial development is realizable. The hinge mechanism was originally designed to improve the alignment of flip-chip capacitors on ceramics substrates. The alignment error observed using older equipment was more than 15  $\mu\text{m}$  in almost all cases. The hinge mechanism was designed to make the receiving module visible in the same image as the host structures such that the alignment was set using a standard probe station. As a result, the alignment error could be reduced or even eliminated if desired.

### **9.2.2 Advantages**

As previously mentioned, flip-chip assembly has not been widely adopted due to the severe disadvantages of the process. The latching off-chip hinge mechanism allows designers to assemble flip-chip structures without specialized equipment and with little or no complex preprocessing. In short, the developed technique is fast, simple, reliable, repeatable, and inexpensive whereby highly advanced MEMS and integrated microsystems can be created with little more than a standard probe station.

Another benefit to this process is the fact that flip-chip structures can be rotated off the edge of the modules during release or the following rinse in methanol. Since many of these structures do not have opposing plates with large surface area, the rotated features can simply be dried in air rather than in the critical point dryer as is necessary with most surface-micromachined structures.

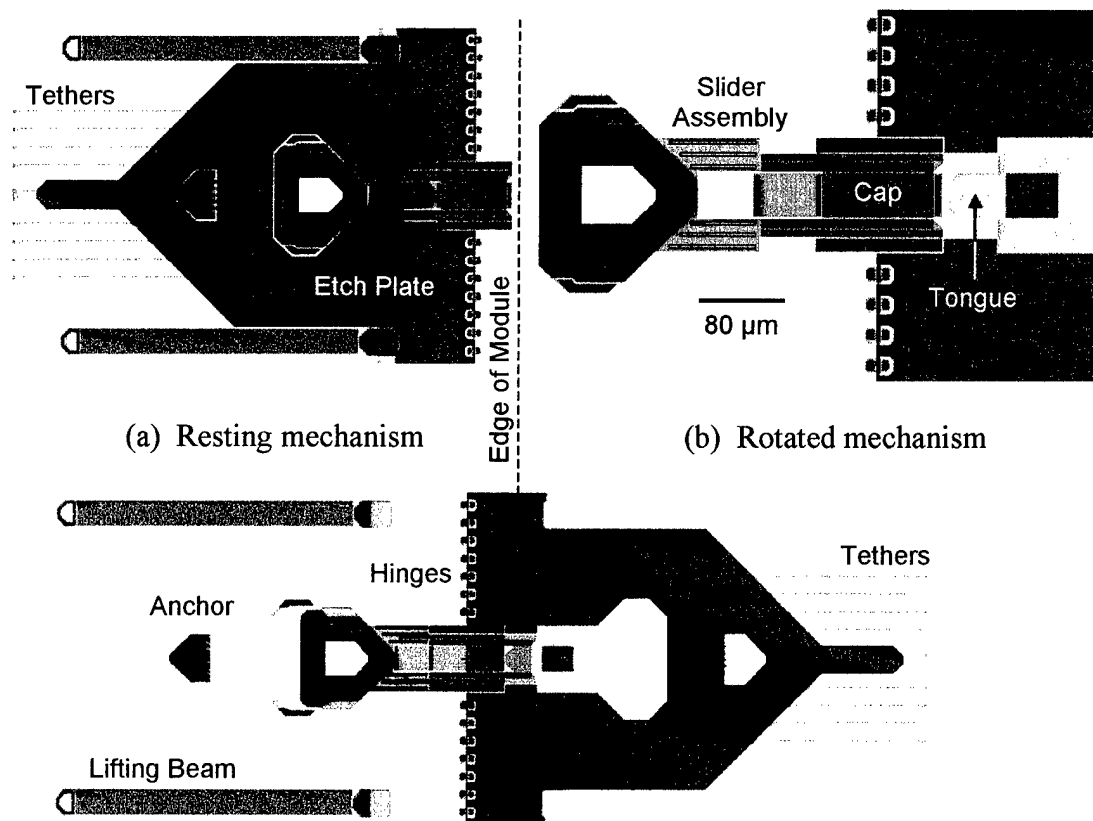
### **9.2.3 Disadvantages**

One of the primary disadvantages of the proposed research is the reliance on the design of surface-micromachined features that enable the flip-chip bonding of other structures. The hinge mechanism and related components must be fabricated on the same host chips next to the structures intended to be flip-chip assembled on other surfaces. The disadvantage comes in two forms. First, the working area available on the host chip decreases since the bonding structures must be placed adjacent to the flip-chip structures. As a result, some advanced layouts may require significant optimization. Additionally, unless working structures are copied from other designers, each new designer must create these features which have the potential to malfunction if not properly designed thereby disabling the technique.

### **9.2.4 Implementation**

The latching off-chip hinge mechanism is formed using only the upper two layers of the MUMPs process. Each feature within the mechanism is carefully designed with specific topographical considerations such that all mating elements align properly when rotated and no object interferes with the motion of any other. Figure 9-5(a) shows the actual layout of a recent design of the hinge mechanism and shows four distinct features. The etch plate is connected to a line of hinges and rigidly supports the tethers that connect to the flip-chip devices to be rotated off the edge of the chip. The lifting beams are simply passive bimorph actuators of polysilicon and gold that are used to initially elevate the arrays. The thermal

mismatch between the two layers results in an upward force at the end of the beam once the module is released. The free end of the beams are placed near the hinges in order to maximize the lifting effect so that the flip-chip structures are sufficiently elevated to use probe tips to complete the rotation. The etch plate is designed to be larger than the largest flip-chip structure so that it is the last feature on the surface of the host module to be released and therefore the only structure to bear the force of the lifting beams. Otherwise, delicate features like micromirror flexures would likely break before the surface is fully released.



(c) Rotated and latched mechanism supporting structures off the edge of the module.

**Figure 9-5.** Illustration of latching off-chip hinge mechanism design and operation.

In order to use the same chips in a variety of bonding techniques, the lifting beams are countered by an anchor that is used to hold the mechanism down. The anchor is connected to the etch plate by thin tethers that are designed to be removed by a laser cutter or burned off when a potential is applied between the anchor and the small pad adjacent to it. Likewise, the tethers connecting the etch plate to the flip-chip structures are designed to be removed in the same manner. A small divot in the end of these tethers concentrates either the mechanical stress or current density at a point along the edge of the flip-chip structures. However, a laser cutter has proven to be the best method of removing nearly all forms of tethers. The anchor tethers are cut to facilitate off-chip hinge bonding while the flip-chip tethers are severed for use in the flip-chip bonding machine using the baseline bonding technique.

The slider assembly is shown in greater detail in Figure 9-5(b) which shows the latching features of the hinge mechanism. The assembly is topographically designed using a vertical spacer plate to elevate the tongue and cap during fabrication. Once rotated, the tongue must rest beneath the cap so that the two features mate when the slider assembly is engaged. The slider assembly is designed with multiple stops to prevent excessive motion that may damage the rotated etch plate.

After the release etch, the hinge mechanism is rotated and latched into position using a standard micromanipulator on a probe station or even by hand holding a probe tip after some practice. The flip-chip structures formed in the upper layers are then ready for bonding on a receiving module using solder, indium or a variety of conductive adhesives. Figure 9-5(c) shows the mechanism in the latched

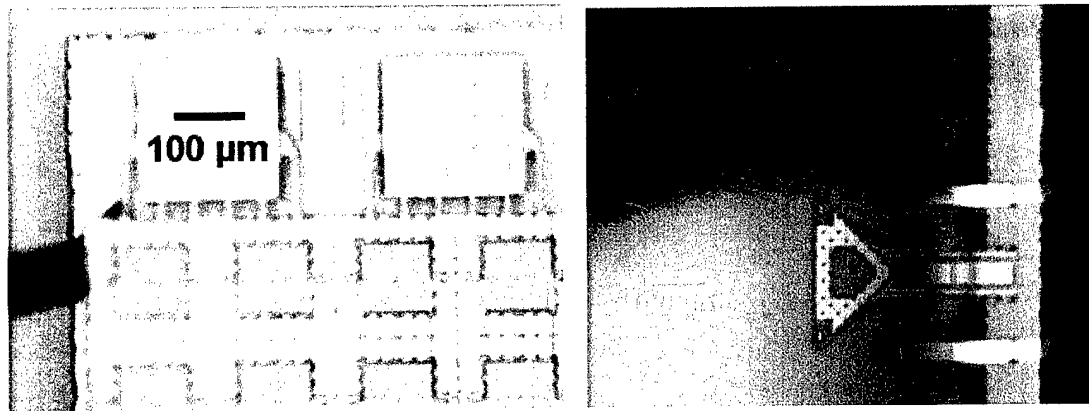
position and illustrates an additional pad connected to the tongue that must occasionally be used to level the etch plate before the slider assembly is engaged.

With the anchor tethers cut, the lifting beams provide sufficient elevation such that numerous arrays have been easily rotated off the edge of the module using only the fluid resistance of methanol during the release rinse. However, great care must be taken when removing the structure from the rinse to avoid surface tension damage to the delicate arrays. Most micromirror arrays can then simply be dried in air rather than using a critical point dryer since they no longer rest above the substrate that would ordinarily damage the mirror surfaces as the methanol evaporates.

Several techniques to raise the hinge mechanism off the host module were adapted from previous research. The first is a small beam that is placed beneath the surface to be raised. One end of the beam is anchored while the other is fashioned with fingers intended to receive a probe tip. The bending of this lifting fork structure has been shown to easily erect small devices or individual micromirrors. It was quickly concluded, however, that much larger lifting forks are capable of raising the entire mechanism about as well as a flock of bricks can fly. All future designs of the lifting forks were immediately abandoned in favor of absolutely anything else.

The most effective technique uses the lifting beams shown in Figure 9-5 which are simply passive bimorph actuators of polysilicon and gold. The thermal mismatch between the two layers results in an upward force at the end of the beam once the module is released. The free end of the beams are placed near the hinges in order to maximize the lifting effect so that the flip-chip structures are sufficiently elevated to use probe tips to complete the rotation.

After release, the flip-chip structures can be rotated off the edge of the chip using a basic micromanipulator. As shown in Figure 9-6(a), however, a probe tip held by hand can be reliably used after gaining some degree of proficiency.

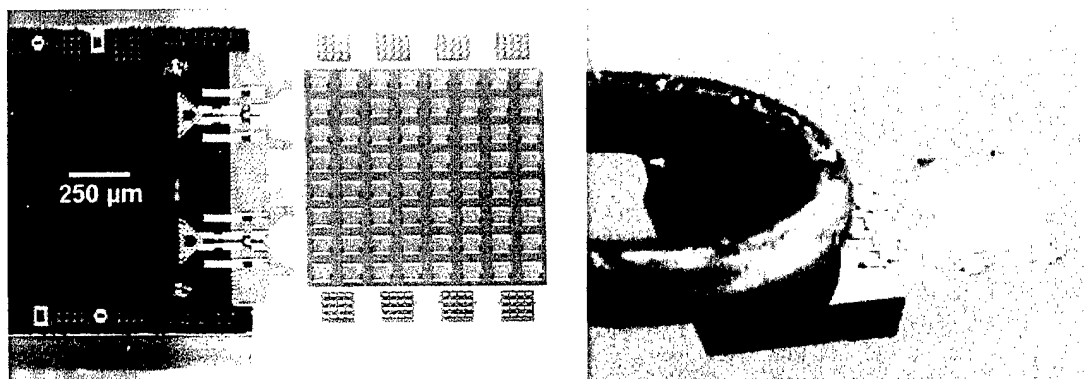


(a) Lifting of array by probe tip

(b) Rotation of array through vertical

**Figure 9-6.** Photographs of typical lifting and rotation of off-chip hinge structures.

The lifting beams are visible in Figure 9-6(b) as the array is rotated through the vertical position. Figure 9-7(a) also shows the beams next to the slider assembly.



(a) Rotated micromirror array

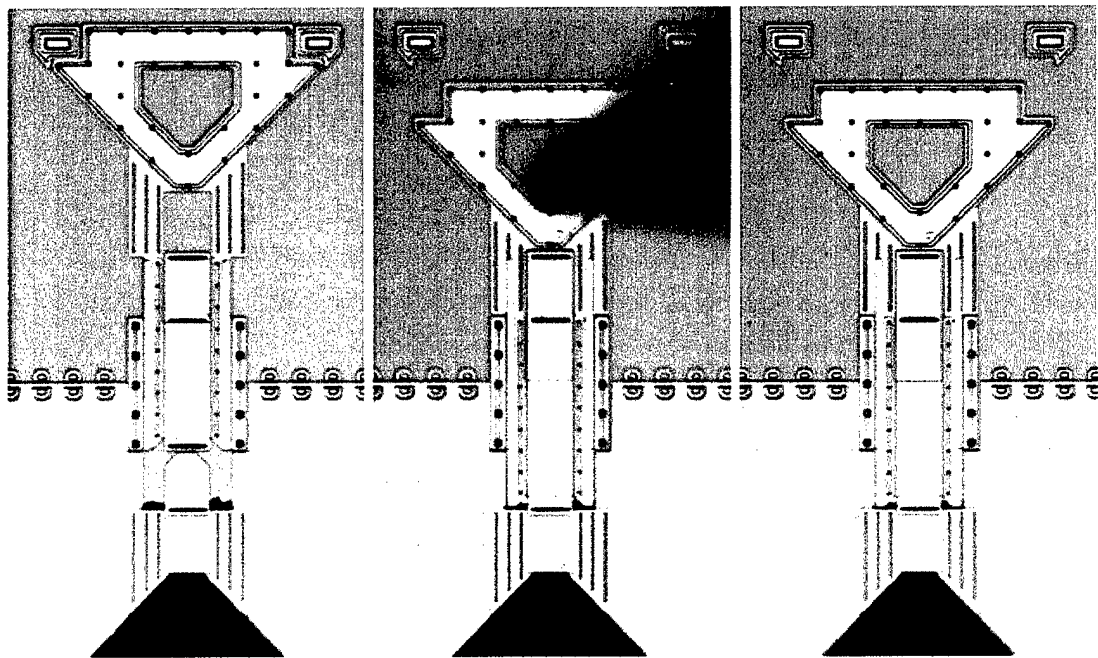
(b) Mounted host module

**Figure 9-7.** Photographs of rotated micromirror array and mounted host module.



Once the arrays are rotated off the edge of the module and latched into position, the host module must be prepared for bonding. As rudimentary as it seems, the best technique for doing so is shown in Figure 9-7(b) in which an epoxy is applied to a flexible wire and attached to the host module. This technique also allows for course position and rotation correction during the bonding process.

Figure 9-8 illustrates the latching sequence showing the original design of the hinge mechanism. The diced edge of the flip-chip module can barely be seen under the tongue of the rotated etch plate.

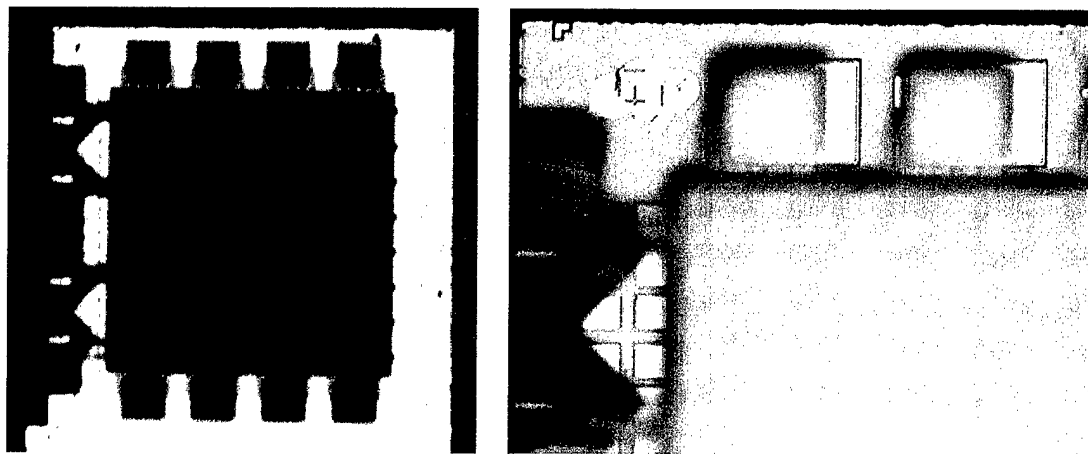


**Figure 9-8.** Photographs of slider assembly latching sequence.

The hinge mechanism shown in Figure 9-8 was the first version to be fabricated and demonstrated only one adverse characteristic. The oxide layer between the polysilicon layers forming the etch plate was intentionally trapped to stiffen the

structure. Unfortunately, the resulting stress was sufficient to slightly warp the plates and occasionally jam the hinges during rotation. Improved designs, as shown in Figure 9-5, use shorter lines of hinges and exposed oxide in the etch plates.

Although rotation and translation controls are quite obvious under the microscope of the probe station, the planarity between the rotated structures and the receiving module is slightly more difficult to sense. Figure 9-9 illustrates typical micromirror alignment over a receiving module using the off-chip hinge assembly.



(a) View of poor planar alignment

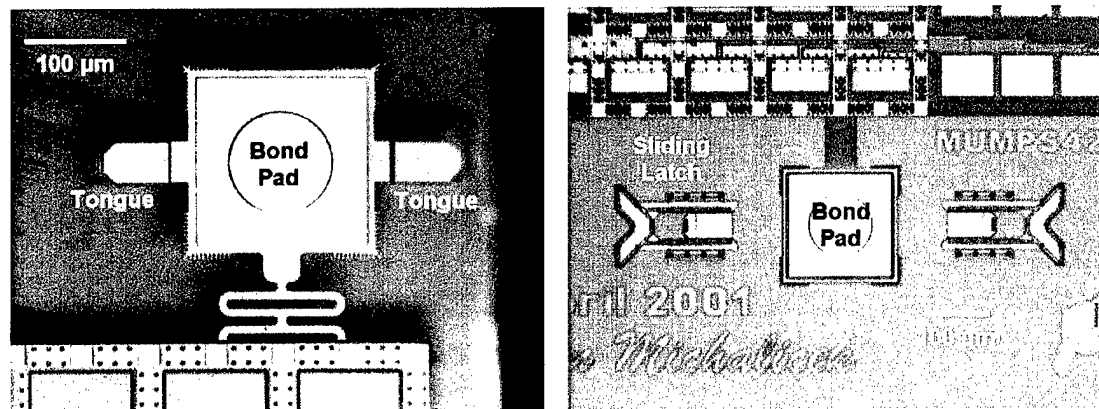
(b) View of proper planar alignment

**Figure 9-9.** Photographs of planar alignment using the off-chip hinge mechanism.

As indicated in Figure 9-9(a), the opposing features on the two modules show a noticeable contrast in lighting when the planar alignment between modules is poor. Under a low magnification objective, the focal depth is such that the light source does not illuminate both features unless they show reasonable alignment. As shown in Figure 9-9(b), the opposing features are relatively parallel and ready for bonding. Using this technique, several micromirror arrays were easily aligned such that the

angle formed between the two planar surfaces was sufficiently small to enable bonding. The elasticity of the bond pads and the flexures supporting them enabled any variance in the planarity to be neglected when pressed into contact with the opposing features on the receiving module.

Probably the easiest means to bond flip-chip features to a receiving module is the use of latches similar to those used in the hinge mechanism. Figure 9-10(a) shows a bond pad of a host module array that has been elevated by lifting beams.



(a) Elevated host bond pad

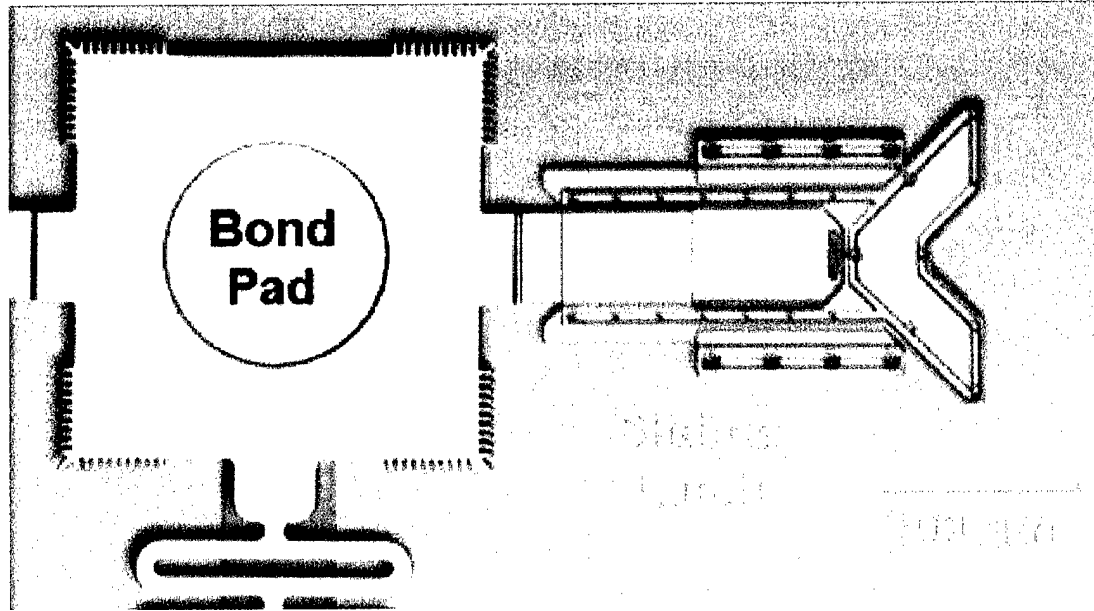
(b) Receiving bond pad

**Figure 9-10.** Photographs of host and receiving portions of a latching bond pad..

The tongues are fabricated above spacer layers so that the two features are positioned well below the bond pad once the array is rotated and positioned above the receiving module. As shown in Figure 9-10(b), the corresponding bond pad on the receiving module has the sliding latch that will capture the tongues of the host bond pad.

The array on the host module is aligned to the receiving module using the probe station controls and lowered into place where the two bond pads make contact. While held with one probe, another probe is used to slide the latches into place.

Again, this can be done by hand after some practice and the alignment accuracy is simply a matter of preference. Figure 9-11 shows a closer view of this sliding latch mechanism in which the host module bond pad rests on a gold-to-gold contact with the receiving module bond pad.



**Figure 9-11.** Photograph of a sliding bond pad latch mechanism.

The alignment error observed with this and most latched arrays has been approximately 1-2  $\mu\text{m}$  for each bond pad pair. The bond pads are connected to the arrays by rounded flexures to allow for added elasticity during the alignment and bonding process. Unfortunately, this also allows each bond pad to demonstrate an alignment error independently of the other bond pads. Ultimately, the main flip-chip structures show minimal alignment error.

One noticeable drawback to this approach was found to be a simple design error. These pads were copied and adapted from the larger 200  $\mu\text{m}$  pads used in the

standard flip-chip process in which large gold surfaces are thermo-compression bonded to each other with little regard for warping. Using this technique, however, the pads are free to deform under the induced stress of thermal mismatch between the polysilicon and the gold layers on the bond pads. As a result, the proper alignment and latching of some pads was somewhat more difficult than others. To eliminate this problem, the latching bond pads should be designed just large enough to enable proper latching and some gold-to-gold contact between pads.

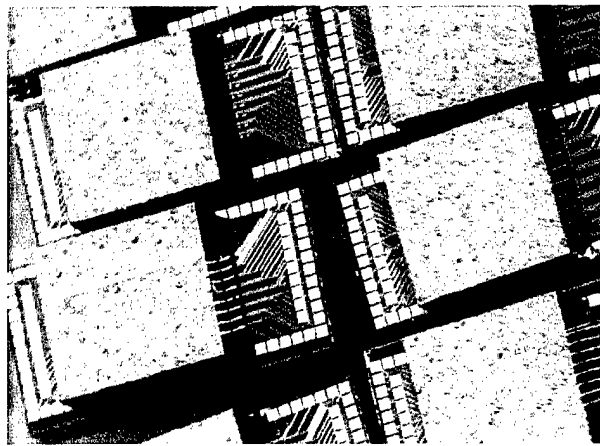
It is this type of off-chip hinge assembly that will enable simple and accurate bonding of flip-chip structures. Since the alignment errors of standard flip-chip assembly are due to the inability to view the structure through the silicon substrate, the off-chip hinge will allow full-time visual alignment during the bonding process and should enable repeatable accuracy within 1-2  $\mu\text{m}$  of lateral error.

### **9.2.5 Compatibility with Standard Process**

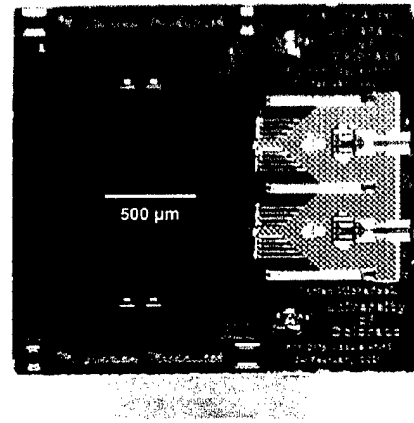
As previously described, the fabrication of flip-chip devices using the latching off-chip hinge mechanism must be compatible with the standard flip-chip bonding process where any flip-chip module can be used in either technique. The anchor shown in Figure 9-5 enables this compatibility such that the hinge mechanism is not lifted off the substrate after the release etch. If the lifting beams were able to do so, it is likely that the delicate micromirror devices or other flip-chip structures would be damaged by the hinge mechanism which supports the weight of the host substrate.

The standard thermo-compression flip-chip bonding process can still be used if the tethers supporting the structures are severed prior to bonding. As previously

described, a laser cutter has become the technique of choice since the tethers can be trimmed close to the arrays, the process is relatively simple and easy to use, and it poses less risk to the arrays than burning them off or simply breaking them. Once the tethers to the arrays are cut, the module is plasma cleaned and bonded using the flip-chip bonding machine just as standard flip-chip modules. Figure 9-12(a) shows several typical bonded modules fabricated in the standard flip-chip process.



(a) Typical bonded modules



(b) Spent host module

**Figure 9-12.** Photograph of bonded modules and spent flip-chip host module.

After flip-chip bonding, the modules are released to free the structures and to discard the original host substrate. It is this release process that is inherently risky for flip-chip structures if lifting beams or other off-chip hinge mechanisms remain on the surface of the host module. The anchor that supports the hinge mechanism helps prevent damage such that the host module slides off the receiving module once all oxide has been removed. Figure 9-12(b) shows a typical spent host module after the flip-chip bonding process. The lines along which the laser cutter was used to separate

the array from the host module can be seen at the ends of the tethers. Ultimately, this advanced form of off-chip hinge mechanism allows a greater number of flip-chip modules to be bonded using a wider variety of flip-chip fabrication methods.

### **9.2.6 Ongoing Research**

With the advent of the off-chip hinge mechanism comes several interesting concepts which are currently being developed. First, if the off-chip bonding process works so well for transferring the layers from a single host module, then far more advanced structures can be built by transferring the layers from multiple host modules. As a result, very tall and highly complex structures can be formed with virtually any number of material layers.

Additionally, true three-dimensional assembly could be realized in which the structures from the host module are bonded to the receiving module at various angles to the substrate rather than parallel to the surface. In this manner, a variety of shapes and complex vertical structures could be formed that would otherwise not be possible with standard surface-micromachined features.

Finally, the latching hinge mechanism could provide a stable platform for the off-chip operation of structures that are not intended for flip-chip assembly. For instance, various optical components, microgrippers, and many types of sensors must be erected or otherwise freed from the original host substrate in order to function, but still require some sort of rigid support assembly. The latching hinge mechanism could be used to hold the devices off the edge of the chip in order to successfully interact with the desired medium.

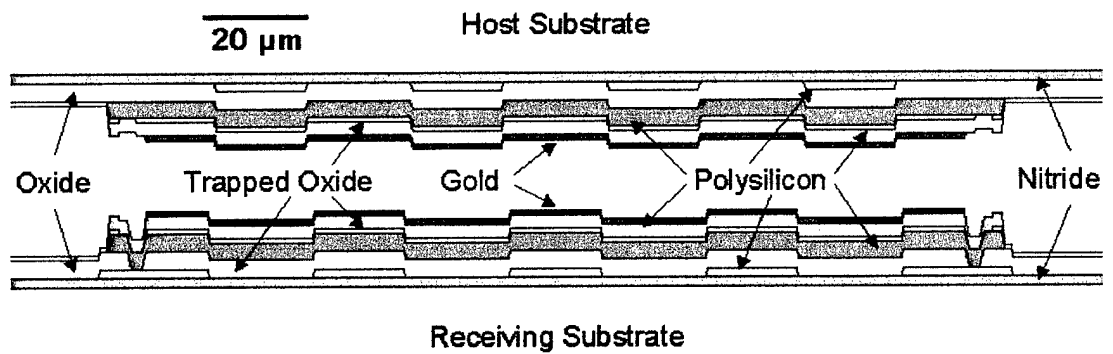
### **9.2.7 Conclusions**

This research has demonstrated a novel and quite versatile latching off-chip hinge mechanism that solves many of the problems associated with standard flip-chip assembly and also uniquely enables a number of new techniques. Micromirror arrays fabricated using this feature have demonstrated inherent planarization, minimal alignment error, as many as five structural layers, mask-free metallization, and simple rotation of flip-chip structures during the release etch. This off-chip mechanism is almost ideally suited to creating a wide variety of integrated microsystems by which the MEMS flip-chip structures are bonded atop a CMOS chip. Ultimately, this mechanism enables a fast, simple and inexpensive means to create highly advanced MEMS and integrated microsystems without specialized equipment or complex preprocessing.

## **9.3 Topographically Opposed Bond Pads**

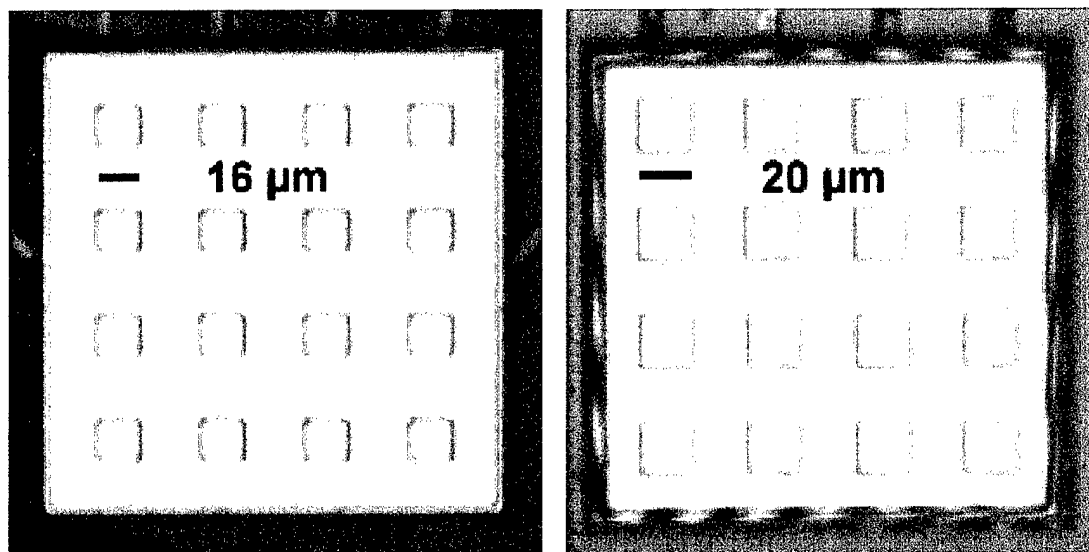
One of the easiest means to improve bonding yield is to correct for slight alignment errors between flip-chip modules during the bonding process. Topographically opposed bond pads were designed for this purpose in which bumps in the bond pad of the host substrate are designed to fit into recessed holes in the bond pad of the receiving substrate. Figure 9-13 illustrates this design and shows that the host substrate bond pad is anchored only by the oxide that is removed during the release etch.





**Figure 9-13.** Cross section view of topographically opposed bond pad layouts.

The gold layers of both pads are equally displaced throughout the entire bond pad such that entire surface area of the pads is used for bonding. Figure 9-14 shows a photograph of both bond pads in which the topographical features are clearly visible.

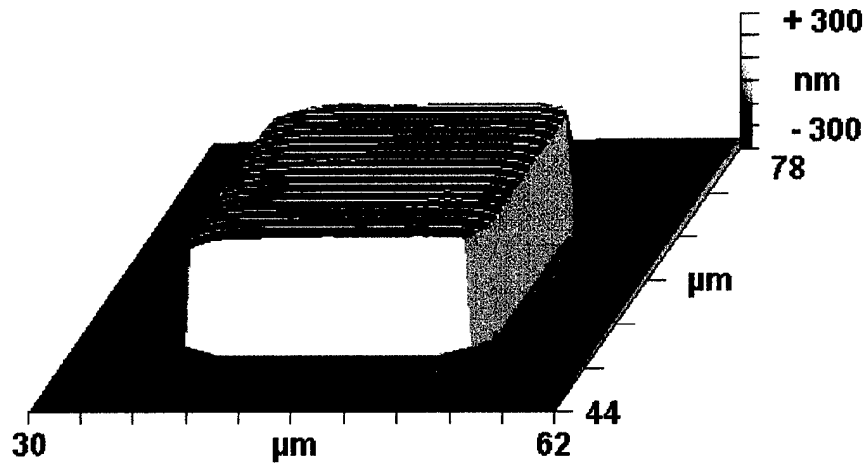


(a) Host pad with upward dimples

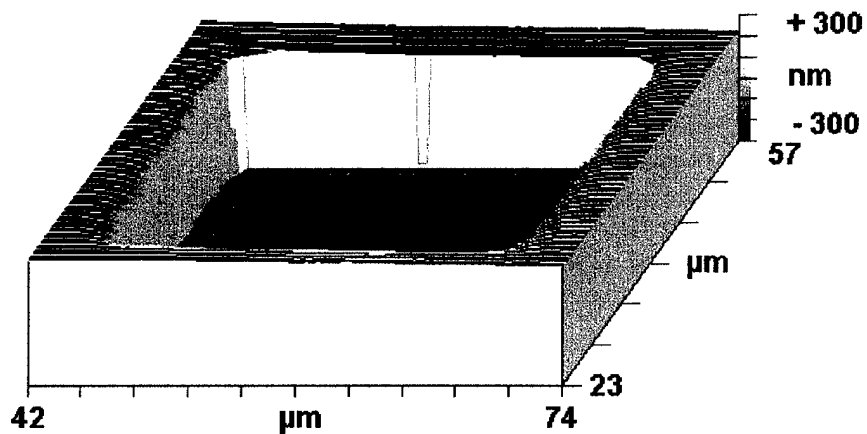
(b) Receiving pad with downward dimples

**Figure 9-14.** Photographs of topographically opposed flip-chip bond pads.

The Zygo interferometric microscope was used to measure these features to ensure proper tolerance in alignment and bonding contact between the bond pads. Figure 9-15 shows the surface relief maps of an upward and downward dimple that are designed to snap together.



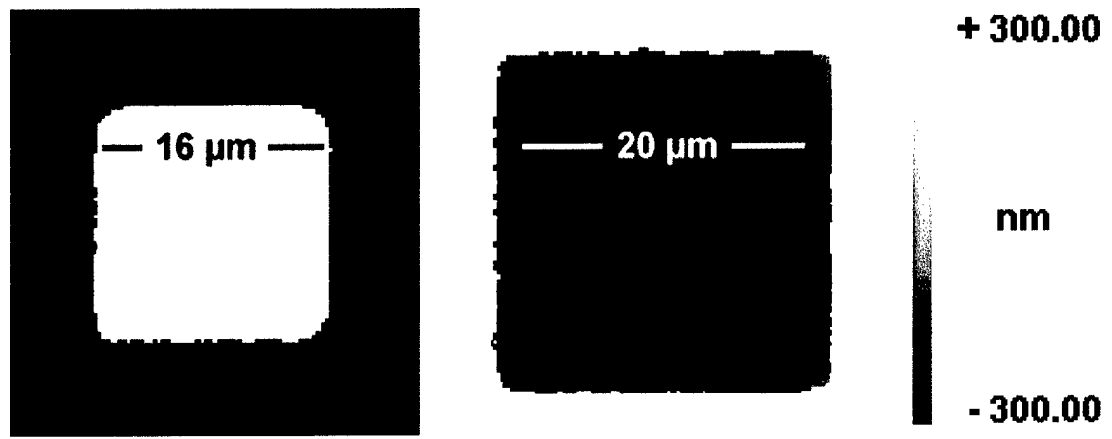
(a) Upward dimple of host substrate bond pad



(b) Downward dimple of receiving substrate bond pad

**Figure 9-15.** Surface relief maps of upward and downward bond pad dimples.

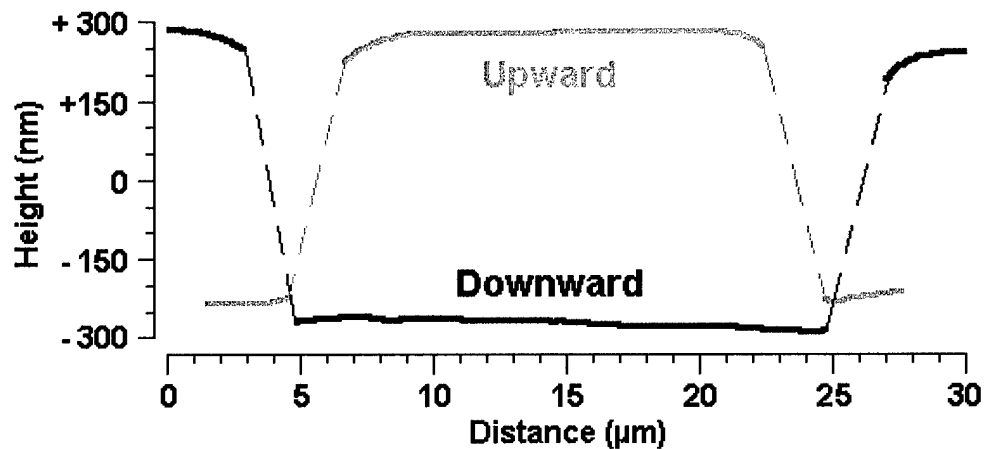
Likewise, the contour plots in Figure 9-16 more clearly show the relative size of each feature in which the upward dimple has approximately a 2  $\mu\text{m}$  clearance around each edge once inserted into the downward dimple of the receiving chip bond pad.



(a) Upward dimple of host pad      (b) Downward dimple of receiving pad

**Figure 9-16.** Contour maps of upward and downward bond pad dimples.

Figure 9-17 illustrates a surface profile through the center of each device and shows the interaction of the dimples along with the total vertical clearance of the features.

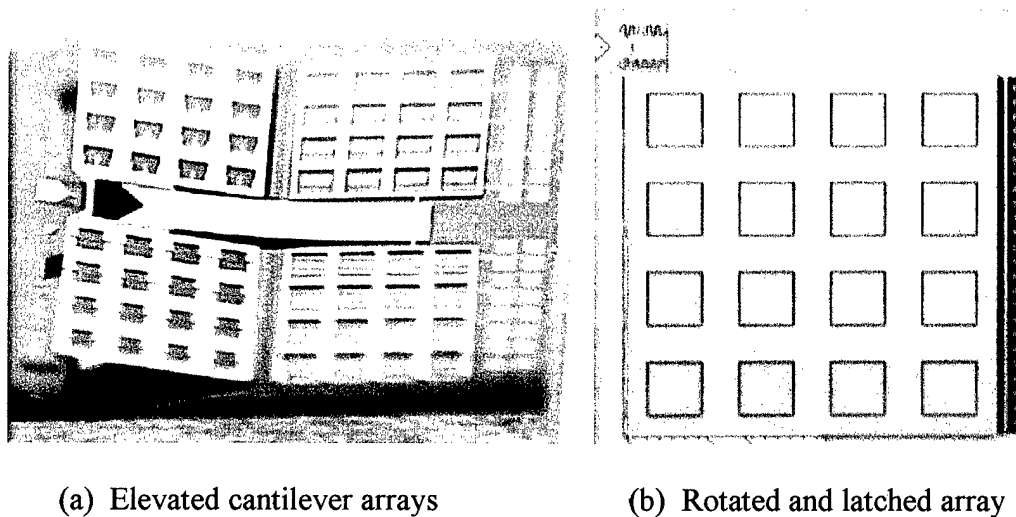


**Figure 9-17.** Surface profile of upward and downward bond pad dimples.

As a result of these features, the lateral alignment error between flip-chip modules has been reduced from an average of approximately 4-5  $\mu\text{m}$  to approximately 2  $\mu\text{m}$  even when counting the few modules that were so poorly aligned that the dimples did not engage the opposing feature. In this case, the modules typically separate before release since only the surface area of the bumps make contact with the opposing pad. In this manner, the topographically opposed bond pads not only enable better alignment, but prevent failed bonds by allowing a poorly aligned bond to be separated and bonded again after calibrating the bonding machine.

## 9.4 Monolithic Flip-Chip Bonding

Another interesting form of flip-chip assembly is the monolithic approach in which the receiving structures are fabricated on the same module as the host structures. Figure 9-18 shows typical monolithic arrays before and after bonding.



**Figure 9-18.** Photographs of two typical monolithic flip-chip cantilever arrays.

As shown in Figure 9-18(a), two released cantilever arrays are initially elevated above the substrate by a passive bimorph polysilicon/gold actuator that lifts the array during the release etch. These arrays are consistently rotated into position during the methanol rinse. Once rotated, as shown in Figure 9-18(b), the arrays are secured by mechanical latches or epoxy such that the final array is very similar to those fabricated by standard flip-chip assembly, but with far fewer process steps. The only disadvantage to this process is that there is no rigid bond supporting the array and some devices have been observed to vibrate the entire array when actuated at higher frequency. The squeeze-film damping of air within the arrays most likely contributes to the motion of the remaining devices.

## **9.5 Summary**

This chapter has described several characteristics and methods of created advanced MEMS and integrated microsystems that are not limited to any one form of flip-chip bonding. The off-chip hinge mechanism, topographically opposed bond pads, and monolithic assembly techniques can be applied to any number of similar flip-chip fabrication projects and will likely produce similar benefits such as the highly planarized surface of flip-chip assembled structures.

## **CHAPTER 10**

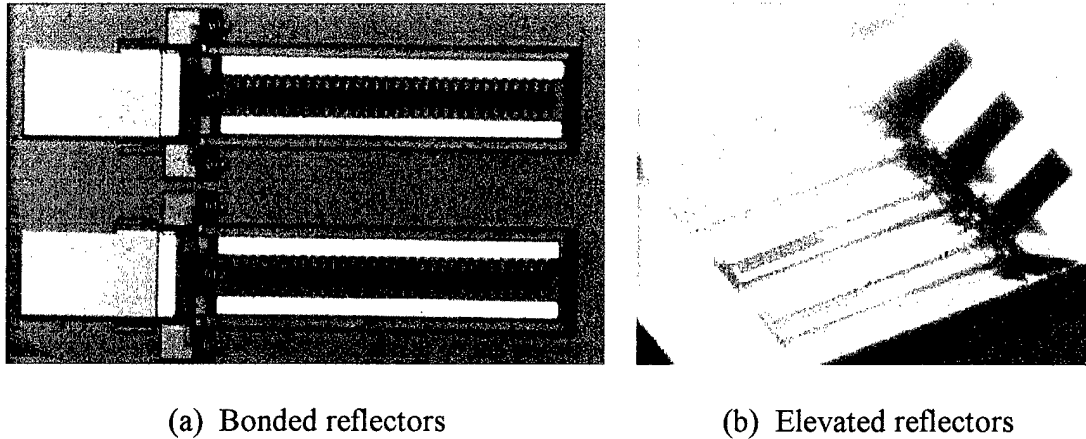
### **SUMMARY AND FUTURE RESEARCH**

As presented in the preceding chapters, flip-chip assembly has been demonstrated as a viable and even more promising means to create advanced MEMS and integrated microsystems that may not be achievable using conventional fabrication methods. There is no doubt that flip-chip fabrication will continue to be explored for the creation of even more advanced devices. Toward that end, many demonstration devices were fabricated in the last few weeks of this research in an effort to interest other researchers in the abilities of flip-chip assembly. Some of these devices are presented in this chapter in order to generate interest in continuing to develop the flip-chip assembly technique for a large number of projects at the University of Colorado at Boulder.

#### **10.1 VCSEL Integration Devices**

A number of researchers are working on Vertical Cavity Surface Emitting Laser (VCSEL) projects who require a means to integrate the vertical beam with other components placed off the edge of the chip. Using the flip-chip assembly process, a few basic structures can be fabricated on the surface of the chip and then

used to receive flip-chip structures to build an adjustable reflector above the laser. For instance, the structures shown in Figure 10-1 were created by bonding a simple reflector plate atop a surface-micromachined structure that is capable of lifting the base plate to a desired angle approximately  $45^\circ$  from the substrate.



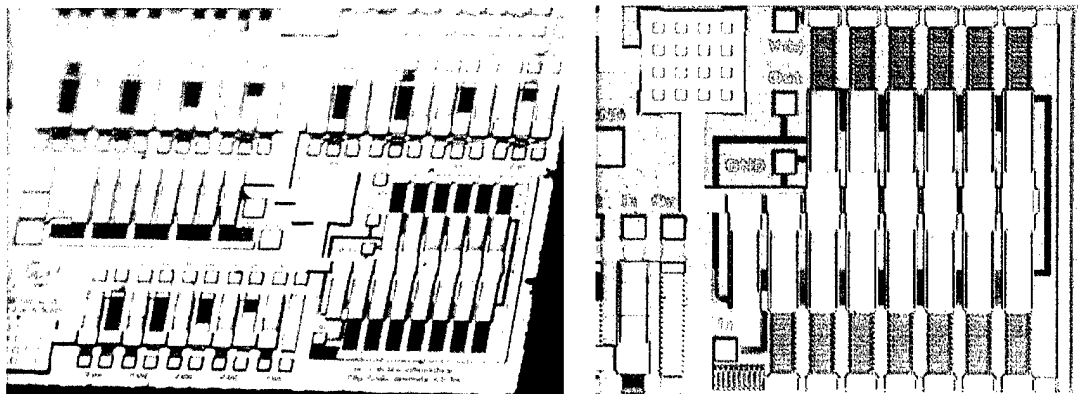
**Figure 10-1.** Photographs of several flip-chip VCSEL integration reflectors.

The structures in Figure 10-1(a) are shown immediately after the bonding process while the structures shown in Figure 10-1(b) have been tuned to the desired angle.

The support beams of the structure shown in Figure 10-1(a) are long bimorph beams comprised of polysilicon and gold layers that will deflect upward due to thermal mismatch stress induced between these layers. The ends of these beams are placed beneath the inner edge of the receiving plate so that this plate will be elevated when the beams are allowed to bend. Small tethers built down the middle of these beams secure them in place such that the beams are elevated in small increments when these tethers are cut using a laser cutter. The devices shown in Figure 10-1(b) were bonded, released and elevated with very little difficulty.

## 10.2 Mechanical Transistors

Given the need for advanced computing technology that does not rely on conventional electronics, a wide variety of digital and analog logic structures were created using mechanical transistors. The receiving module shown in Figure 10-2(a) contains a variety of AND, OR, XOR, and Inverter structures along with their natural inverted counterparts. These structures are electrostatically actuated such that the same basic logic structures are realized as in CMOS electronics. Therefore, any larger, more complex logic circuit can be created using these building blocks.



(a) Wide view of numerous logic structures

(b) Close view of ring oscillator

**Figure 10-2.** Photographs of several flip-chip mechanical transistor logic structures.

The ring oscillator shown in Figure 10-2(b) demonstrated that these transistors can be employed in series such that the output of one device can effectively drive the input of others. Based on the performance of this circuit, it is obvious that the future development of such flip-chip devices is a highly promising means to realize very simple, low-cost and reliable mechanical computing components.



One of the biggest advantages to this type of fabrication is that the structures are fabricated with gold/gold bonds and adjustable contacts. The mechanical transistors are capable of passing a significant amount of current through the gold layer running between the source and drain contacts of the device. This inherent feature of flip-chip assembly using the MUMPS process is just one of the benefits available to designers of advanced MEMS components.

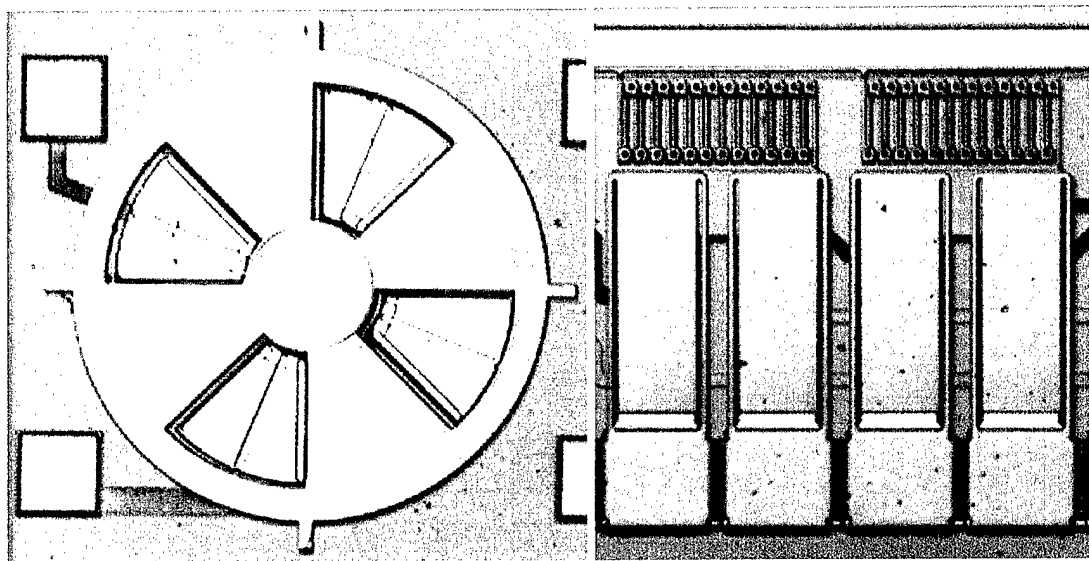
### **10.3 Miniaturized Capacitors and Mechanical Relays**

Similar to the mechanical transistors, a variety of capacitors, latches, relays, and other miniaturized conventional electrical components have been fabricated using flip-chip assembly. For instance, one of several flip-chip fabrication techniques could be used to assemble high-voltage relays atop CMOS control electronics. The relays can be simple cantilever style latches that are designed to collapse at a very specific voltage. The drive electrode formed in the CMOS layers can be maintained at the system voltage until the relay is engaged at which point the drive electrode switches to ground. The small potential difference between the two plates is only sufficient to snap the relay once the drive electrode is grounded. In this manner, standard CMOS electronics chips could be used to drive very high-voltage or even high-power loads without special fabrication services or even complicated interconnects and amplifiers.

Taking this design even further, any number of conventional devices or mechanical switches can be miniaturized and easily integrated onto CMOS electronics or simply to other mechanical circuits. Flip-chip assembly can be used in

place of complicated packaging technologies that have previously been used to integrate such devices without directly coupling them to each other. This approach to directly fabricating miniaturized components will lead to the development of truly advanced MEMS and highly integrated microsystems.

As shown in Figure 10-3(a), a basic design of variable capacitor can be created with opposing gold plates and wiring such that the device can obtain a high Q factor at reasonable frequencies. This device is simply a rotating plate that varies the amount of surface area overlapping the lower plate.



(a) Conventional rotating variable capacitor      (b) Mechanical latches and relays

**Figure 10-3.** Photographs of other demonstration flip-chip structures.

Similar to the transistors, the mechanical relays shown in Figure 10-3(b) can be fabricated to make gold/gold contacts for high-power connections or numerous cross-connecting switches. Although the behavior of such a device is very sensitive to the

flexures and other design considerations, the flip-chip assembly of such mechanical switching elements has produced numerous working devices.

## **10.4 Summary**

In recent years, the flip-chip fabrication of advanced MEMS and integrated microsystems has been demonstrated with a variety of devices and almost as many techniques to create even more unique and previously unrealizable systems. Whether by thermocompressive bonding, monolithic bonding, or off-chip hinge bonding, the flip-chip fabrication techniques presented in this dissertation will no doubt enable a variety of fast, low-cost, simple, and reliable yet high-performance components that were previously unavailable. The devices created as part of this research are only a small fraction of what will be developed as emerging applications drive future designs. Ultimately, the wide variety of flip-chip techniques developed to produce these devices will certainly be used to create many of them.

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## **APPENDIX A**

### **VARIABLE CAPACITOR CALCULATOR CODE**



```
{ Variable Capacitor Calculator }
{ Written by M. Adrian Michalick }
{ Version 1.2 Edited 12 July 1999 }
```

VERSION 4.00

```
Begin VB.Form frmVCaps
    Caption           = "Variable Capacitors"
    ClientHeight      = 7500
    ClientLeft        = 1425
    ClientTop         = 1620
    ClientWidth       = 11055
    Height            = 7905
    Left              = 1365
    LinkTopic         = "Form1"
    ScaleHeight       = 7500
    ScaleWidth        = 11055
    Top               = 1275
    Width             = 11175
    Begin VB.TextBox txtInputFile
        Height         = 285
        Left           = 2700
        TabIndex       = 19
        Text           = "C:\Users\Michalick\VCaps\Constants.txt"
        Top            = 1800
        Width          = 5655
    End
    Begin VB.TextBox txtSpringConstants
        Height         = 6795
        Left           = 8580
        MultiLine      = -1 'True
        TabIndex       = 17
        Top            = 540
        Width          = 2295
    End
    Begin VB.CommandButton cmdClearData
        Caption        = "Clear Data"
        Height         = 555
        Left           = 6900
        TabIndex       = 16
        Top            = 1080
        Width          = 1455
    End
    Begin VB.TextBox txtNumPoints
        Alignment       = 2 'Center
        Height          = 285
        Left           = 7620
        TabIndex       = 14
        Text           = "500"
        Top            = 540
        Width          = 735
    End
    Begin VB.TextBox txtSnapHeight
        Alignment       = 2 'Center
        Height          = 285
        Left           = 2700
        TabIndex       = 11
        Text           = "0.5"
        Top            = 540
        Width          = 735
    End
    Begin VB.TextBox txtRestingHeight
        Alignment       = 2 'Center
```

```

        Height      = 285
        Left        = 2700
        TabIndex    = 10
        Text        = "3.5"
        Top         = 120
        Width       = 735
    End
    Begin VB.CommandButton cmdCalculate
        Caption      = "Calculate"
        Height       = 555
        Left        = 5100
        TabIndex    = 9
        Top         = 1080
        Width       = 1455
    End
    Begin VB.TextBox txtDeviceArea
        Alignment    = 2 'Center
        Height       = 285
        Left        = 2700
        TabIndex    = 8
        Top         = 960
        Width       = 735
    End
    Begin VB.TextBox txtConstantRange
        Alignment    = 2 'Center
        Height       = 285
        Left        = 2700
        Locked       = -1 'True
        TabIndex    = 6
        Top         = 1380
        Width       = 1635
    End
    End
    Begin VB.PictureBox picPlotFrame
        BackColor    = &H00FFFFFF&
        Height       = 4560
        Left        = 180
        Picture      = "VCaps.frx":0000
        ScaleHeight  = 300
        ScaleMode    = 3 'Pixel
        ScaleWidth   = 541
        TabIndex    = 4
        Top         = 2760
        Width       = 8175
    End
    End
    Begin VB.TextBox txtOutputFile
        Height       = 285
        Left        = 2700
        TabIndex    = 3
        Text        = "C:\Users\Michalicek\VCaps\Character.csv"
        Top         = 2220
        Width       = 5655
    End
    End
    Begin VB.TextBox txtNumDevices
        Alignment    = 2 'Center
        Height       = 285
        Left        = 7620
        Locked       = -1 'True
        TabIndex    = 0
        Top         = 120
        Width       = 735
    End
    End
    Begin VB.Label lblLabels
        Caption      = "Constants Output File:"
    End

```

```

BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
    Name           = "MS Sans Serif"
    Size           = 8.25
    Charset        = 0
    Weight         = 700
    Underline      = 0 'False
    Italic         = 0 'False
    Strikethrough  = 0 'False
EndProperty
Height           = 255
Index           = 1
Left            = 180
TabIndex       = 20
Top            = 1860
Width          = 2655
End
Begin VB.Label lblLabels
    Caption       = "Spring Constants ( N/m ):"
    BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
        Name           = "MS Sans Serif"
        Size           = 8.25
        Charset        = 0
        Weight         = 700
        Underline      = 0 'False
        Italic         = 0 'False
        Strikethrough  = 0 'False
    EndProperty
    Height        = 255
    Index         = 8
    Left          = 8580
    TabIndex      = 18
    Top           = 180
    Width         = 2235
End
Begin VB.Label lblLabels
    Caption       = "Number of Points to Plot:"
    BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
        Name           = "MS Sans Serif"
        Size           = 8.25
        Charset        = 0
        Weight         = 700
        Underline      = 0 'False
        Italic         = 0 'False
        Strikethrough  = 0 'False
    EndProperty
    Height        = 255
    Index         = 7
    Left          = 5100
    TabIndex      = 15
    Top           = 600
    Width         = 2655
End
Begin VB.Label lblLabels
    Caption       = "Initial Resting Separation:                μm"
    BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
        Name           = "MS Sans Serif"
        Size           = 8.25
        Charset        = 0
        Weight         = 700
        Underline      = 0 'False
        Italic         = 0 'False
        Strikethrough  = 0 'False
    EndProperty

```

```

        Height      = 255
        Index       = 6
        Left        = 180
        TabIndex    = 13
        Top         = 180
        Width       = 3915
    End
    Begin VB.Label lblLabels
        Caption      = "Snap Down Separation:                μm"
        BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
            Name      = "MS Sans Serif"
            Size      = 8.25
            Charset   = 0
            Weight    = 700
            Underline  = 0 'False
            Italic    = 0 'False
            Strikethrough = 0 'False
        EndProperty
        Height      = 255
        Index       = 5
        Left        = 180
        TabIndex    = 12
        Top         = 600
        Width       = 3915
    End
    Begin VB.Label lblLabels
        Caption      = "Device Surface Area:                μm^2"
        BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
            Name      = "MS Sans Serif"
            Size      = 8.25
            Charset   = 0
            Weight    = 700
            Underline  = 0 'False
            Italic    = 0 'False
            Strikethrough = 0 'False
        EndProperty
        Height      = 255
        Index       = 4
        Left        = 180
        TabIndex    = 7
        Top         = 1020
        Width       = 3915
    End
    Begin VB.Label lblLabels
        Caption      = "Spring Constant Range:                N/m"
        BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
            Name      = "MS Sans Serif"
            Size      = 8.25
            Charset   = 0
            Weight    = 700
            Underline  = 0 'False
            Italic    = 0 'False
            Strikethrough = 0 'False
        EndProperty
        Height      = 255
        Index       = 3
        Left        = 180
        TabIndex    = 5
        Top         = 1440
        Width       = 4935
    End
    End
    Begin VB.Label lblLabels
        Caption      = "Behavior Output File:"

```

```

BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
    Name           = "MS Sans Serif"
    Size           = 8.25
    Charset        = 0
    Weight         = 700
    Underline      = 0 'False
    Italic         = 0 'False
    Strikethrough  = 0 'False
EndProperty
Height           = 255
Index           = 2
Left            = 180
TabIndex       = 2
Top            = 2280
Width          = 2655
End
Begin VB.Label lblLabels
    Caption       = "Number of Devices:"
    BeginProperty Font {0BE35203-8F91-11CE-9DE3-00AA004BB851}
        Name           = "MS Sans Serif"
        Size           = 8.25
        Charset        = 0
        Weight         = 700
        Underline      = 0 'False
        Italic         = 0 'False
        Strikethrough  = 0 'False
    EndProperty
    Height        = 255
    Index         = 0
    Left         = 5100
    TabIndex     = 1
    Top          = 180
    Width        = 2655
End
End
Attribute VB_Name = "frmVCaps"
Attribute VB_Creatable = False
Attribute VB_Exposed = False
'C:\Users\Michalicek\VCaps\Constants.txt
'C:\Users\Michalicek\VCaps\Character.csv
'C:\VisBasic\projects\VCaps\Constants.txt
'C:\Visbasic\projects\VCaps\Character.csv

Private Sub cmdCalculate_Click()

    Const Epsilon = 8.854188 * 10 ^ -12
    Const Precision = 0.0001
    Const StartDelta = 0.1
    Const VoltBuffer = 1.1

    Const LeftMargin = 53
    Const TopMargin = 20
    Const PlotWidth = 460
    Const PlotHeight = 240

    Dim Delta As Double
    Dim Springs() As Double
    Dim Resting, Snap, Area As Double
    Dim MaxVolt, OldDisp, NewDisp As Double
    Dim Sample, OldSample, NewSample As Double
    Dim Capacitance, Potential As Double
    Dim MinConst, MaxConst As Double
    Dim Index, Point As Integer

```

```

Dim NumDevices, NumPoints As Integer
Dim TempString As String
Dim RootFound As Boolean

Dim PlotX, PlotY, PlotBuffer As Integer

Dim Slope, D1, D2 As Double

picPlotFrame.Refresh

Open txtInputFile.Text For Output As #1
Print #1, txtSpringConstants.Text
Close #1

NumDevices = 0
Open txtInputFile.Text For Input As #1
While Not EOF(1)
    Line Input #1, TempString
    If Val(Trim(TempString)) > 0 Then
        ReDim Preserve Springs(NumDevices + 1)
        Springs(NumDevices) = Val(Trim(TempString))
        NumDevices = NumDevices + 1
    End If
Wend

Close #1

MinConst = Springs(0)
MaxConst = Springs(0)
For Index = 2 To NumDevices
    If Springs(Index - 1) > MaxConst Then MaxConst = Springs(Index - 1)
    If Springs(Index - 1) < MinConst Then MinConst = Springs(Index - 1)
Next Index

If MaxConst * 1000 - Int(MaxConst * 1000) < 0.5 Then
    MaxConst = Int(MaxConst * 1000) / 1000
Else: MaxConst = Int(MaxConst * 1000 + 1) / 1000
End If

If MinConst * 1000 - Int(MinConst * 1000) < 0.5 Then
    MinConst = Int(MinConst * 1000) / 1000
Else: MinConst = Int(MinConst * 1000 + 1) / 1000
End If

txtNumDevices.Text = Str(NumDevices)
If MinConst < 1 Then TempString = "0" Else TempString = ""
TempString = TempString + Str(MinConst) + " < k < "
If MaxConst < 1 Then TempString = TempString + "0"
txtConstantRange.Text = TempString + Str(MaxConst)

NumPoints = Val(txtNumPoints.Text)
Resting = Val(txtRestingHeight.Text)
Snap = Val(txtSnapHeight.Text)
Area = Val(txtDeviceArea.Text)

'Calculations for sloped resting position:
D1 = Resting
D2 = Resting * 4

Open txtOutputFile.Text For Output As #1
Print #1, ""
Print #1, ",Number of Devices:,,,"; Str(NumDevices)
Print #1, ",Number of Points:,,,"; Str(NumPoints)

```

```

Print #1, ",Device Surface Area:,,,"; Str(Area); ", $\mu\text{m}^2$ "
Print #1, ",Resting Separation:,,,"; Str(Resting); ", $\mu\text{m}$ "
Print #1, ",Snap Down Separation:,,,"; Str(Snap); ", $\mu\text{m}$ "
Print #1, ",Permittivity Constant:,,,"; Str(Epsilon); ",F/m"
Print #1, ""

Potential = Sqr(MinConst / (Epsilon * Area)) / 1000
' Potential = Potential * ((2 / 3) * Resting) ^ (3 / 2)
Potential = Potential * ((2 / 3) * D1) ^ (3 / 2)

MaxVolt = Sqr(MaxConst / (Epsilon * Area)) / 1000
' MaxVolt = MaxVolt * ((2 / 3) * Resting) ^ (3 / 2)
MaxVolt = MaxVolt * ((2 / 3) * D2) ^ (3 / 2)

Index = Int(Potential * (NumPoints - 1) / (VoltBuffer * MaxVolt)) + 1
Point = Int((NumPoints - 1) / VoltBuffer)

TempString = ",Best Fit Linear Slopes:,,,"=Slope(C"
TempString = TempString + Trim(Str(Index + 20)) + ":C"
TempString = TempString + Trim(Str(Point + 20)) + ",B"
TempString = TempString + Trim(Str(Index + 20)) + ":B"
TempString = TempString + Trim(Str(Point + 20)) + ")""

TempString = TempString + ",pF/Volt,"=Slope(G"
TempString = TempString + Trim(Str(Index + 20)) + ":G"
TempString = TempString + Trim(Str(Point + 20)) + ",B"
TempString = TempString + Trim(Str(Index + 20)) + ":B"
TempString = TempString + Trim(Str(Point + 20)) + ")""

Print #1, TempString + ",pF/Volt"

TempString = ",Best Fit Linear Intercepts:,,,"=Intercept(C"
TempString = TempString + Trim(Str(Index + 20)) + ":C"
TempString = TempString + Trim(Str(Point + 20)) + ",B"
TempString = TempString + Trim(Str(Index + 20)) + ":B"
TempString = TempString + Trim(Str(Point + 20)) + ")""

TempString = TempString + ",pF,"=Intercept(G"
TempString = TempString + Trim(Str(Index + 20)) + ":G"
TempString = TempString + Trim(Str(Point + 20)) + ",B"
TempString = TempString + Trim(Str(Index + 20)) + ":B"
TempString = TempString + Trim(Str(Point + 20)) + ")""

Print #1, TempString + ",pF"

Print #1, ""
Print #1, ",Best Fit Curve Offset:,,,0,pF"
Print #1, ",Best Fit Curve Magnitude:,,,"=EXP($G$10)"",pF"
Print #1, ",Best Fit Curve Exponential:,,,"=$G$9"",1/V"
Print #1, ""
Print #1, ",Applied,Total,Best Fit,Best Fit,Total,Curve,Curve"
Print #1, ",Potential,Capacitance,Line,Curve,Capacitance,Data,,Spring
Constants (N/m)"

TempString = ",(Volts),(pF),(pF),(pF),(pF),(pF),(pF),"
For Index = 1 To NumDevices
    TempString = TempString + "," + Str(Springs(Index - 1))
Next Index

Print #1, TempString
Print #1, ""

' Capacitance = (Epsilon * Area / Resting) * 10 ^ 6

```

```
Capacitance = (Epsilon * Area / D1) * 10 ^ 6
```

```
TempString = ",0," + Str(NumDevices * Capacitance) + ","
TempString = TempString + """"=E10""", ""=$G$10^2+$E$12""", ""=C20+$E$12""""
TempString = TempString + ", ""=SQRT(C20)""", ""=$G$9*B20+$G$10""", "
For Index = 1 To NumDevices
    TempString = TempString + ",0"
Next Index
```

```
Print #1, TempString
```

```
' PlotBuffer = Int(PlotHeight / ((Resting / Snap) + 1))
PlotBuffer = Int(PlotHeight / ((D2 / Snap) + 1))
```

```
picPlotFrame.CurrentX = LeftMargin + PlotWidth + 1
picPlotFrame.CurrentY = TopMargin + PlotBuffer
```

```
PlotX = LeftMargin
PlotY = TopMargin + (Resting / Snap) * PlotBuffer
```

```
picPlotFrame.Line -(PlotX, PlotY), RGB(0, 0, 0), B
```

```
picPlotFrame.CurrentX = PlotX + 1
```

```
For Point = 2 To NumPoints
    Capacitance = 0
    TempString = ""
    txtNumPoints.Text = Str(Point)
    Potential = VoltBuffer * ((Point - 1) / (NumPoints - 1)) * MaxVolt
    For Index = 1 To NumDevices
        Delta = StartDelta
        MinConst = Springs(Index - 1)
```

```
'Calculations for sloped resting position:
Resting = D1 + (D2 - D1) * (Index - 1) / (NumDevices - 1)
```

```
Sample = 1000000 * Epsilon * Area * Potential ^ 2
Sample = Sample / (2 * MinConst * Resting ^ 3)
```

```
If Sample < (4 / 27) And Potential < MaxVolt Then
    NewDisp = 0
    RootFound = False
    While Not RootFound
        OldDisp = NewDisp
        OldSample = Sample - OldDisp * (1 - OldDisp) ^ 2
        NewDisp = OldDisp + Delta
        NewSample = Sample - NewDisp * (1 - NewDisp) ^ 2
        If NewSample * OldSample < 0 Then
            RootFound = Abs(NewDisp - OldDisp) < Precision
            Delta = Delta / 10
            NewDisp = OldDisp
        End If
        If NewDisp > 1 / 3 Then
            NewDisp = 0
            Delta = Delta / 10
        End If
    DoEvents
```



```

        Wend
    Else: NewDisp = (Resting - Snap) / Resting
    End If

    If NewDisp / Precision - Int(NewDisp / Precision) < 0.5 Then
        NewDisp = Int(NewDisp / Precision) * Precision
    Else: NewDisp = Int(NewDisp / Precision + 1) * Precision
    End If

    TempString = TempString + "," + Str(NewDisp)
    Capacitance = Capacitance + 1 / (Resting * (1 - NewDisp))
Next Index

TempString = Trim(Str(19 + Point)) + "+G$10","" + TempString
TempString = Trim(Str(19 + Point)) + ")", "" + TempString
TempString = ", ""=SQRT(C" + TempString

TempString = ""=C" + Trim(Str(19 + Point)) + "+E$12"" + TempString

TempString = "+G$10)^2+E$12","" + TempString
TempString = ""=($G$9*B" + Trim(Str(19 + Point)) + TempString

TempString = "*E$9+E$10","" + TempString
TempString = ""=B" + Trim(Str(19 + Point)) + TempString

Capacitance = Capacitance * Epsilon * Area * 10 ^ 6
TempString = "," + Str(Capacitance) + "," + TempString

TempString = "," + Str(Potential) + TempString

Print #1, TempString

PlotX = LeftMargin + (Potential / (MaxVolt * VoltBuffer)) * PlotWidth
Capacitance = Capacitance * Snap / (NumDevices * Epsilon * Area * 10 ^
6)
PlotY = TopMargin + PlotBuffer * ((1 - Capacitance) * (Resting / Snap) +
1)

picPlotFrame.Line -(PlotX, PlotY), RGB(255, 0, 0)

Next Point

Close #1

MsgBox "Characterization Completed!"

End Sub

Private Sub cmdClearData_Click()

    txtSpringConstants.Text = ""
    txtDeviceArea.Text = ""

End Sub

Private Sub Form_Load()

    Dim InputFile, OutputFile As String

    InputFile = "C:\Users\Michalicek\VCaps\Constants.txt"
    OutputFile = "C:\Users\Michalicek\VCaps\Character.csv"

```

```

If Dir(InputFile) = "" Then
    InputFile = "C:\VisBasic\projects\VCaps\Constants.txt"
    txtInputFile.Text = InputFile
End If
If Dir(OutputFile) = "" Then
    OutputFile = "C:\Visbasic\projects\VCaps\Character.csv"
    txtOutputFile.Text = OutputFile
End If

If Dir(InputFile) = "" Then txtInputFile.Text = ""
If Dir(InputFile) = "" Then txtOutputFile.Text = ""

End Sub

```